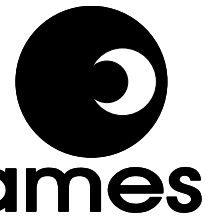


RM410ASEB Application Note: Low-Cost Watt-Hour Energy Meter



RM410ASEB

FEATURES

- n Designed to meet IEC61036 requirements for class 1 active energy meters
- n Selectable rated conditions, LED pulse rates and counter resolutions
- n On-board precision calibration
- n Direct drive capability for stepper motor or impulse counter
- n Opto-isolated output for connection to measurement equipment

INTRODUCTION

This application note addresses various design aspects of a low-cost watt-hour energy meter based on the SAMES SA4104A integrated circuit. The SA4104A is a single-chip solution for accurate bi-directional energy measurement. It incorporates an on-chip oscillator and has a direct drive capability for a stepper motor or an impulse counter. The emphasis for the design of this meter has been placed on meeting the specifications whilst incurring the lowest possible cost. The specification for this design is the International Standards IEC61036 (Alternating current static watt-hour meters for active energy). This meter is designed to meet all class 1 sections of the IEC61036 specification that relate to electrical characteristics.

and converted to the required input current via the current input network. The scaled mains voltage signal is applied to the SA4104A via a voltage divider circuit. Calibration is done by means of a resistive network on the voltage sensing network. Both the current and voltage input networks incorporate low-pass filters to improve the meters performance, especially the immunity to electromagnetic disturbances. The measured energy is displayed on a stepper motor or an impulse counter. An LED as well as an optical isolator provide an electrically isolated connection to measurement equipment during calibration and performance verification.

METER SPECIFICATIONS

A basic meter block diagram using the SA4104A is shown in Figure 1. The load current is sensed with a shunt resistor

The most important IEC61036 class 1 accuracy specifications to which the meter was designed are listed in Table 1 on page 2. The typical value of I_{MAX} is 400% of I_b .

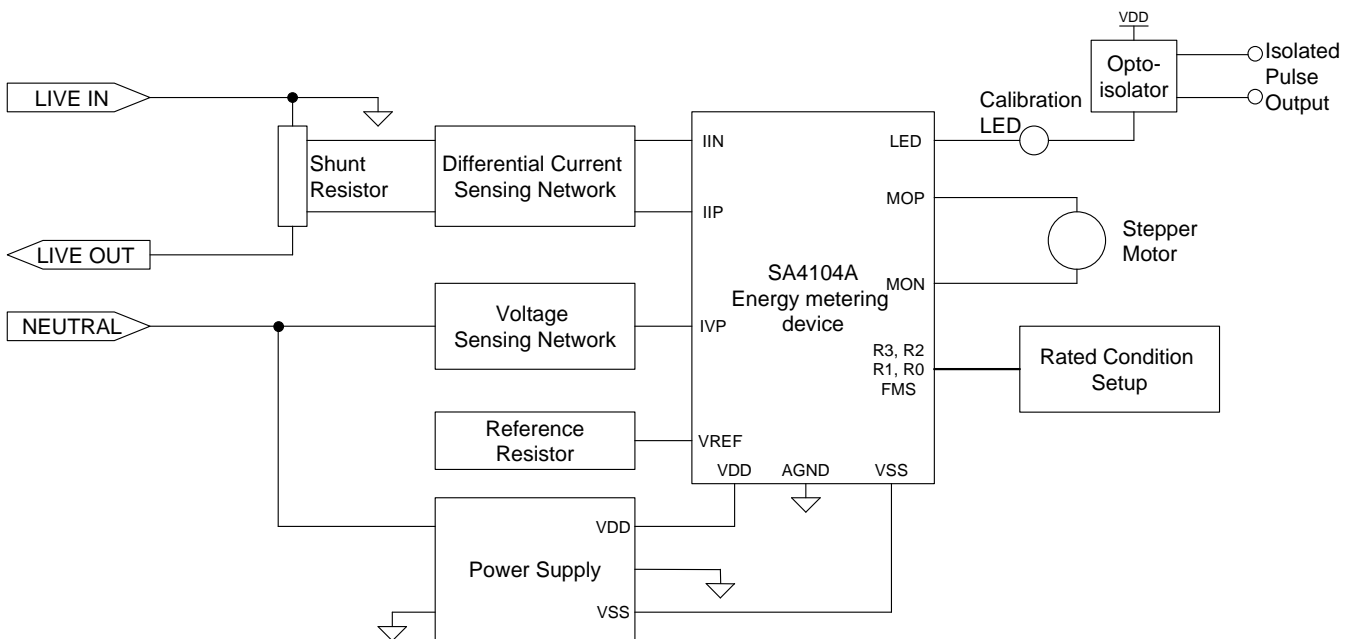


Figure 1: Block diagram of a watt-hour meter based on the SA4104A



Current Value	Power Factor	Class 1 Error Limits
$0.05I_b \leq I < 0.1I_b$	1	$\pm 1.5\%$
$0.1I_b \leq I \leq I_{MAX}$	1	$\pm 1.0\%$
$0.1I_b \leq I < 0.2I_b$	0.5 inductive (lag)	$\pm 1.5\%$
$0.1I_b \leq I < 0.2I_b$	0.8 capacitive (lead)	$\pm 1.5\%$
$0.2I_b \leq I \leq I_{MAX}$	0.5 inductive (lag)	$\pm 1.0\%$
$0.2I_b \leq I \leq I_{MAX}$	0.8 capacitive (lead)	$\pm 1.0\%$

Table 1: IEC61036 Accuracy Specifications

CIRCUIT DESIGN PRINCIPLES CURRENT SENSING NETWORK

The primary function of the current sensing network is to sense the load current and convert it to the input current signal required by the SA4104A. The current sensing network is shown in Figure 2.

The amplitude of the input current into the SA4104A at maximum current (I_{MAX}) should be set as close as possible to $16\mu A_{RMS}$. The current input of the device saturates at $25\mu A$ peak current, so the $16\mu A_{RMS}$ input current ($22.62\mu A$ peak) allows for an over-current up to $110\% I_{MAX}$ before saturation occurs. The SA4104A can be used with most available shunts. To ensure proper current sensing it is advisable to use a shunt that will give a minimum voltage drop of at least 10mV at maximum current. Lower values can also be used, but this could affect the accuracy of the meter at very low load currents. The internal current feedback present on the inputs IIN and IIP of the SA4104A creates a virtual short circuit between these two input pins. This means that the resistor value required to generate the correct input current can be calculated using:

$$R18 = R19 = R20 = R21 = \frac{I_{MAX} \times R_{SH}}{16 \times 10^{-6}} \times \frac{1}{4} = R_C \quad (1)$$

where R_{SH} is the shunt resistance.

A secondary function of the current sense network is to attenuate all high frequency components that could disrupt the accuracy of the SA4104A. These high frequency components may occur due to high frequency surges (fast transient burst), may be induced through strong electric fields or may simply be noise on the power lines. Certain high frequency components, typically those close to integer multiples of the sampling frequency of the analog to digital converters will be mapped close to 50Hz once sampled (a process known as aliasing) and will distort the accuracy of the converters. This can be prevented by adequately attenuating all high frequency signal components. The typical oscillator frequency is 3.58MHz and the analog to digital converters of the SA4104A operate at one half of this frequency, so sufficient attenuation should be present at 1.79MHz. This can readily be achieved by placing a single order RC low pass filter on each current input as shown in Figure 2. The capacitors cannot be placed directly on the input pins IIN and IIP because no differential voltage signal exists between these pins due to the virtual short circuit created by the input network of the SA4104A. The input resistance is therefore split into two equal resistors (R18/R20 and R19/R21) and the capacitor is placed between these resistors. Now a differential voltage can appear across the capacitors and hence filter high

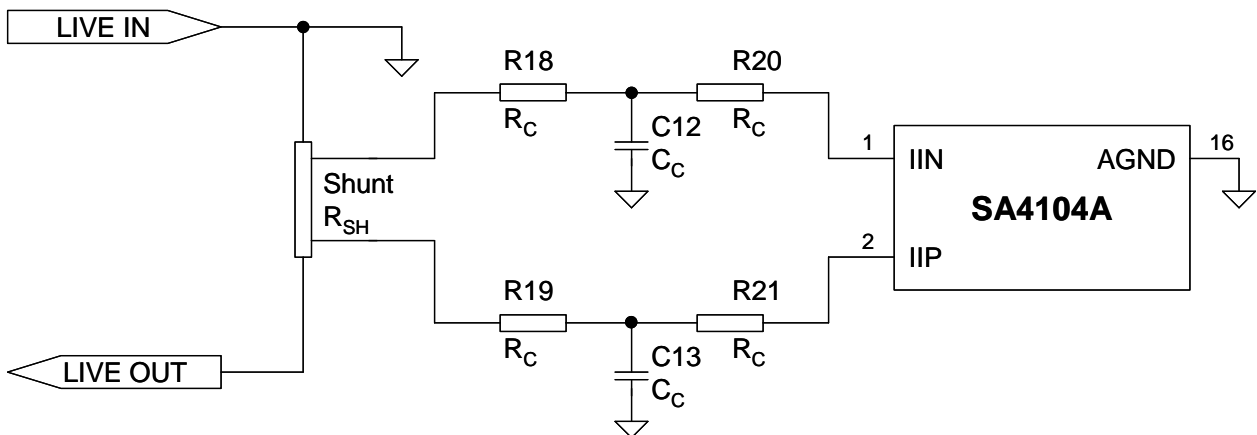


Figure 2: Circuit diagram of the current sensing network



frequencies. The lowest -3dB cut-off frequency is achieved when all four input resistors are equal ($R18 = R19 = R20 = R21 = R_C$). The current input networks must be balanced so both capacitors C12 and C13 must also be equal ($C12 = C13 = C_C$). In this case the equivalent resistance associated with each capacitor is $\frac{1}{2}R_C$ and the -3dB cut-off frequency is

$$f_{C,-3dB} = \frac{1}{\pi R_C C_C} \quad (2)$$

This frequency should be somewhere between 10kHz and 20kHz to ensure both adequate attenuation at integer multiples of the analog to digital converters sampling frequency, and very low phase shift at mains frequency and its harmonics. The requirement for the very low phase is explained under the "Voltage Sense Network" section.

VOLTAGE SENSING NETWORK

The voltage sensing network performs similar functions to the current sensing network. It senses the mains voltage and converts it to the input current signal required by the SA4104A. It also filters all unwanted signals and prevents them from distorting the performance of the SA4104A. The voltage sensing network is shown in Figure 3.

The voltage sensing network is composed of an adjustable voltage divider (resistors R6 to R16) and the current input resistor that generates the required current input signal for the SA4104A. The first consideration when designing the voltage sensing network is that the -3dB cut-off frequency has to be very closely matched to that of the current sensing network. This is important to ensure that the phase shift experienced by the voltage and current signals is identical. If this is not the case the energy meter will have poor performance under non-unity power factor load conditions. The high cut-off frequency of the input network filters does ensure that this matching does not have to be extremely precise. This allows component tolerances to be accommodated without seriously affecting the performance of the meter. The best matching between the cut-off frequencies is achieved by using identical capacitors on both the current and voltage sensing networks, so C11 should equal C12 and C13. The IVP input is a virtual short circuit to analog ground (AGND) so the equivalent resistance associated with C11 is

$$R_{equ-C11} = R16 \parallel R17 \parallel R_X \quad (3)$$

where R_X is the series combination of R6, R7 and R_{trim} . Further, R_{trim} is the series combination of the resistors R8 to R15 that can be enabled or disabled to calibrate the meter. If both R_X and R17 are designed to be significantly larger than R16 then

$$R_{equ-C11} \approx R16 \quad (4)$$

To match the -3dB cut-off frequency of the Current Sensing Network R16 should therefore equal $\frac{1}{2}R_C$ which is the value of the current sense network equivalent resistance. This ensures balanced phase shifts on the current and voltage input networks so the performance of the meter at non-unity power factors will not be affected.

The voltage input IVP of the SA4104A has to be driven with a current of $11\mu A_{RMS}$ at the nominal rated mains voltage. This input also saturates at $25\mu A$ peak current, so the $11\mu A_{RMS}$ input current allows for 50% overdrive capability while maintaining linearity. This ensures that the device will not saturate with a $\pm 20\%$ variation in mains voltage. The simplest method is to set the input resistor R17 at 100 times the value of R16, so it will not significantly affect the -3dB cut-off frequency of the voltage sense network. Setting

$$R17 = 100 \times R16 = 50R_C \quad (5)$$

sets the required output voltage on the voltage divider to

$$V_D = 11 \times 10^{-6} \times 100 \times R16 \quad (6)$$

because the IVP pin has a virtual short to ground. Given that R17 and R_X are large compared to R16

$$V_D = \frac{R16}{R16 + R_X} \times V_{NOM} \approx \frac{R16}{R_X} \times V_{NOM} \quad (7)$$

Combining these equations results in

$$R_X = \frac{V_{NOM}}{11 \times 10^{-4}} \approx 909 V_{NOM} \quad (8)$$

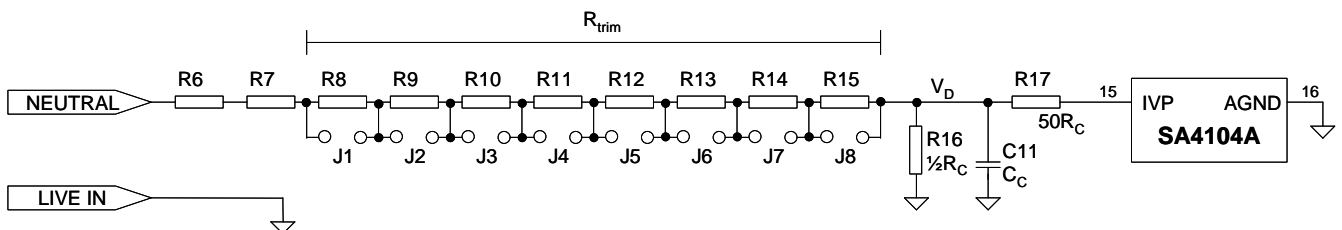


Figure 3: Circuit diagram of the voltage sensing network



which should easily satisfy the condition that R_x should be significantly larger than R16. It must be noted that R_x changes during calibration of the meter, so if the stated condition is not met, the -3dB cut-off frequency of the voltage sensing network will change during calibration of the meter which is not desirable.

A calibration mechanism is required to compensate for component tolerances. The SA4104A and the shunt resistor are the components that will exhibit the widest tolerances. The combination of these two can have variations in the order of $\pm 10\%$. All resistors should be 1% metal film resistors so that the resistor tolerance is low and can be ignored. The total tuning range is therefore 20%. A binary weighted series combination of eight resistors will therefore allow calibration to an accuracy of $20\%/256 = 0.78\%$ which is considered sufficient for a low-cost class 1 energy meter. To achieve approximately 10% tuning range in either direction around the nominal point the highest resistance in the calibration network (R8) should therefore be 10% of R_x with each subsequent resistor having half the value of the previous one. The values of the voltage divider and calibration network are then designed using

$$R6 + R7 = R_x - 10\%R_x = 0.9R_x, \quad (9)$$

$$R9 = 10\%R_x, \quad (10)$$

$$R9 = 0.5 \times R8, R10 = 0.5 \times R9, R11 = 0.5 \times R10, \text{ etc} \quad (11)$$

This topology of current and voltage input networks has some advantages for mass production. The first is that the value of R_x which is used to determine the calibration network is independent of R16. This is important because the value of R16 is half that of the current input resistors (R18 to R21) which will be specific to the shunt. The shunt can therefore be changed without having to adapt the calibration network, i.e. the calibration network is universal. Secondly, one of the input networks can be used to intentionally introduce a phase shift between the voltage and the current signal networks by reducing the cut-off frequency. This allows phase shift compensation to be performed for certain shunts that may exhibit phase shift due to high shunt inductance.

SA4104A RELATED CIRCUITRY

All aspects discussed in this section are illustrated on the complete meter schematic (Figure 6). The SA4104A requires a split supply of +2.5V (VDD) and 2.5V (VSS) around the meter ground node, which has to be connected to the AGND pin of the SA4104A. These three supply lines have to be properly decoupled using capacitors C8 and C9 (220nF ceramic each) between the supplies and ground and C10 (1 μ F ceramic) between the two supplies. These capacitors are required to achieve good performance and have to be

placed as close to the device as possible. Their placement is as important as their presence, placing them more than a few millimeters away from the device renders them useless. The on-chip reference current is derived from a 47k Ω resistor (R22) connected between VREF and VSS. This resistor must be a 1% tolerance metal film type or similar. The metal film ensures that less noise will be induced into the device pin. A 220nF ceramic capacitor (C14) must also be connected between the VSS side of the resistor and ground for noise filtering the reference current.

The internal pulse dividers of the SA4104A are configured through the pins R3, R2, R1, R0 and FMS. These pins must either be tied to VDD or VSS. The FMS pin can be left floating to enable a fast pulse output mode which is typically not applicable to a low-cost energy meter of this type. These setup pins can be directly connected to VDD or VSS, no pull-up or pull-down resistors are required.

The stepper motor used to display the consumed energy should be connected to the MOP and MON pins through two small current limiting resistors (R24 and R25). For calibration and performance verification purposes an LED and opto-isolator are connected in series to the LED output pin of the SA4104A. This output is active low so the LED and opto-isolator are connected through a current limiting resistor to VDD.

For more elaborate information on setting up and using the SA4104A, refer to the SA4104A datasheet available on the SAMES website at www.sames.co.za or from any SAMES representative.

SETUP OF R0, R1, R2, R3 AND FMS FOR DIFFERENT RATED CONDITIONS

The following equations and table state the basic pulse constants and motor constants obtainable with the SA4104A.

The pulse rate of the LED output is:

$$p/kWh_{LED} = \frac{IVP}{16} \times 5000 \times \frac{1}{DF_{LED}} \times \frac{3600 \times 1000}{V_{NOM} \times I_{MAX}} \quad (12)$$

where IVP is the input current to the SA4104A at V_{NOM} . For $V_{NOM} = 220V$ this should typically be 11 μ A.

The motor output pulse rate is

$$p/kWh_{MOTOR} = p/kWh_{MOTOR} \times \frac{1}{DF_{MO}} \quad (13)$$



The variables DF_LED and DF_MO are defined by setting FMS, R0, R1,R2 and R3 according to Table 2.

FMS	R3	R2	R1	R0	DF_LED	DF_MO
0	0	0	0	0	220	256
0	0	0	0	1	440	128
0	0	0	1	0	880	64
0	0	0	1	1	1760	32
0	0	1	0	0	220	128
0	0	1	0	1	440	64
0	0	1	1	0	880	32
0	0	1	1	1	1760	16
0	1	0	0	0	220	64
0	1	0	0	1	440	32
0	1	0	1	0	880	16
0	1	0	1	1	1760	8
0	1	1	0	0	220	32
0	1	1	0	1	440	16
0	1	1	1	0	880	8
0	1	1	1	1	1760	4
1	0	0	0	0	1464	64
1	0	0	0	1	2928	32
1	0	0	1	0	352	64
1	0	0	1	1	704	32
1	0	1	0	0	584	32
1	0	1	0	1	1168	16
1	0	1	1	0	352	32
1	0	1	1	1	704	16
1	1	0	0	0	584	16
1	1	0	0	1	1168	8
1	1	0	1	0	352	16
1	1	0	1	1	704	8
1	1	1	0	0	292	16
1	1	1	0	1	584	8
1	1	1	1	0	234	16
1	1	1	1	1	468	8

Table 2: Division factors available on the SA4104A

'0' indicates that the input is connected to VSS
'1' indicates that the input is connected to VDD

POWER SUPPLY

The RM4104ASEB meter uses a capacitive supply with two zener diode based regulators with series transistors to generate the required +2.5V and -2.5V power supply. The complete power supply circuit is shown in Figure 4. The main consideration behind this type of supply is low cost.

A typical simple single stage zener diode regulator does not have sufficient stability across temperature variations, load current variations and input mains voltage variations to supply the SA4104A with an adequate quality power supply. Furthermore, a typical 2.5V zener diode has a very large series resistance which causes large voltage variations as the load current varies. The series transistor output stage ensures that the zener diode can be biased at almost constant current for varying load current, thereby improving the load regulation of the supply. This is especially important in this application, where the load current can peak when the stepper motor is activated. The V_{BE} of the transistor is now in series with the load so a 3.3V zener diode is chosen. If this diode is biased at a fairly low current (approximately 3mA) the breakdown voltage is approximately 3.1V. Now the 0.6V V_{BE} of the transistor is subtracted and the output voltage of the regulator is 2.5V. The transistors can be any low-cost switching transistors.

The output series transistor configuration improves the load regulation but cannot improve the line regulation characteristic of the regulator. Due to the high on-resistance of a low voltage zener diode the line regulation of the supply is quite poor. Ensuring good line regulation is important because mains voltage variations and the high load current surges can change the input voltage to the rectifier significantly. If the line regulation is poor, the performance of the SA4104A will be affected. To improve the line regulation a second zener diode regulation stage is used. This stage is based on a 5.6V zener that basically creates a fairly stable input voltage for the second regulator stage.

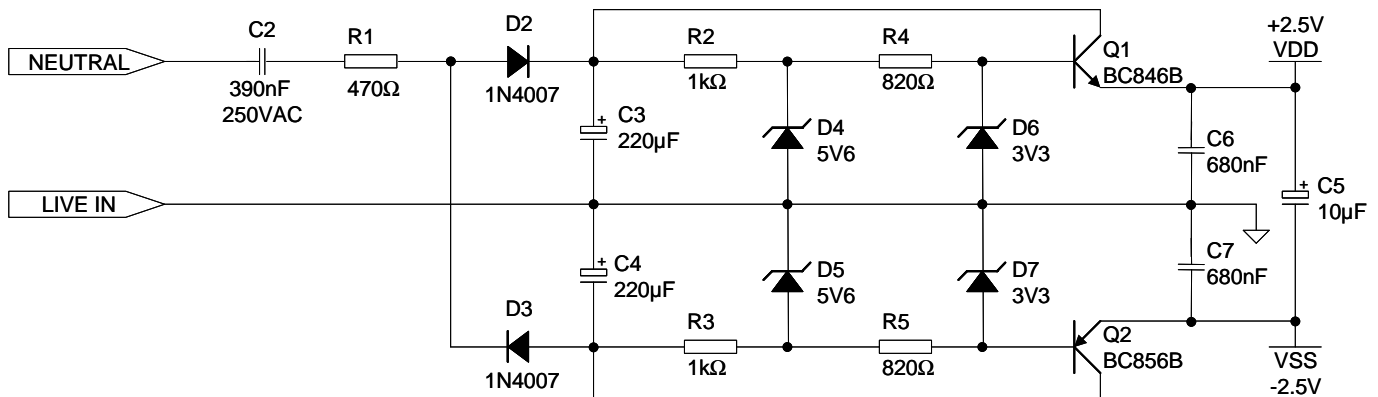


Figure 4: Circuit diagram of the power supply circuit



The output voltage of the first regulator will be close to 5.6V and that of the second stage 3.1V. The 3.3V zener diode should be biased at approximately 3mA so the bias resistors R4 and R5 should be $(5.6V-3.1V)/3mA=820\Omega$. The half-wave rectifier output at nominal load current is typically in the order of 12V. The 5.6V zener diode does not require a very high bias current given that its line regulation is not critical, so a bias current between 2mA and 3mA is sufficient. The bias resistors R2 and R3 should therefore be set at $(12V-5.6V)/5.5mA \approx 1k\Omega$.

The final consideration is the temperature stability of the supply. A 3.3V zener diode typically has a temperature coefficient of $-2mV/^{\circ}C$. The V_{BE} of the output transistor exhibits a similar temperature coefficient, leading to a total temperature coefficient of between $-4mV/^{\circ}C$ and $-5mV/^{\circ}C$. This will cause significant voltage drop over the meter's standard operating range and could lead to accuracy problems on the SA4014A. The 5.6V zener diode on the other hand has a positive temperature coefficient, typically in the order of $+2mV/^{\circ}C$. As the temperature increases the current through R4 and R5 will therefore increase and will cause the output voltage of the 3.3V zener regulator to increase due to the low bias current as well as the high on resistance of the 3.3V zener diode. This configuration almost cancels the temperature coefficient of the output voltage of the regulator.

The series capacitor and resistor (C2 and R1) limit the current drawn from the mains supply and determine the power consumption (VA rating) of the supply. A 390nF capacitor is sufficient to ensure a power supply that operates over a range of $220V\pm 20\%$. In this state the supply consumes about 6VA. If a meter is designed for a lower nominal mains voltage (i.e. 110V) the value of this capacitor has to be scaled accordingly to about 820nF.

Some filtering is required on the output of the supply in the form of two ceramic capacitors (C6 and C7) to ensure that high frequency signals cannot reach the SA4014A through the supply lines. These capacitors should be placed close to the transistors to ensure that noise is filtered at its source. A 10 μ F electrolytic capacitor is required to filter out any low frequency noise spikes in the power supply voltage.

IMMUNITY TO ELECTROMAGNETIC DISTURBANCE

The typical electromagnetic disturbances that can cause the meter to fail or incorrectly record energy are:

- n Electrostatic discharge and surges
- n Electromagnetic HF (high frequency) fields
- n Fast transient burst (FTB)

Typically these disturbances will either cause complete and permanent failure by damaging the sensitive CMOS circuitry of the SA4104A through high voltage levels or cause incorrect registration of energy through high frequency signals that are aliased into the operating bandwidth of the device, thereby disrupting the energy calculation algorithm. The immunity of a class 1 watt-hour meter to these types of disturbances is prescribed by the IEC61036 specification.

Generally two protection mechanisms are required. The first is to ensure that dangerously high voltage levels are sufficiently attenuated or clamped so that no permanent damage can occur to the SA4104A and other sensitive components. To ensure this the complete meter is protected with an MOV S20K275 (Metal Oxide Varistor) to clamp any high voltage potentials. A 10nF capacitor (C1) is placed in parallel with the MOV to ensure that any parasitic inductance that can increase the amplitude and duration of dangerous voltage spikes, is cancelled. The LIVE IN and NEUTRAL inputs are connected directly across the MOV with the lowest possible impedance. With the MOV and C1 in place all extremely high voltage levels are clamped. Typically a larger MOV can absorb more energy and will therefore be more effective at clamping high voltage levels to protect the SA4104A. The subsequent filtering and attenuation of the input networks will also ensure that no damage can occur to the SA4104A by further reducing the Voltage levels that can reach the device.

An MOV alone will not be sufficient to ensure that the meter's performance is not affected by the presence of electromagnetic disturbances during operation. All high frequency signal components need adequate filtering by the filters in the current sensing network, voltage sensing network and the power supply. This should ensure that the meters performance is not affected by the presence of high frequency signals that are directly applied (FTB test) or induced (HF immunity test). The immunity to these types of interference can be improved by reducing the cut-off frequency of the filter networks. This is however only practical to a certain point, before matching between the filters on the voltage and current channel cause linearity issues at non-unity power factor. Alternatively ferrite beads could be used to enhance the filtering, by using them



between the SA4104A and the power supply (in the place of J9, J10 and J11) and on the two shunt connections to the PCB. The voltage input network cannot be protected with a ferrite bead but this is typically not necessary because the attenuation is very high.

Further protection mechanisms are related to the PCB layout and are described in the next section.

PCB DESIGN CONSIDERATIONS

There are numerous PCB design aspects to consider when designing an energy meter using SA4104A. These principles have all been incorporated in the sample PCB layout given in the "PCB Layout" section.

The first is the location of critical components. The current and voltage sensing input resistors (R17 to R21) with their associated low pass filtering capacitors (C11 to C13) should be located as close to the device pins as possible. The same holds for the reference resistor (R22) with its associated filtering capacitor (C14) and the supply bypass capacitors (C8 to C10).

The SA4104A should be placed on a solid ground plane that is connected to the AGND pin of the device. This ground plane should be kept clear of noise by only connecting it to the ground plane of the power supply and the LIVE IN input at a single point. It should also be kept away from any high frequency, high voltage or high current signals that may induce noise. For example, the first section of the voltage input attenuation network (R6 and R7) should be placed far away from this ground plane. If a ferrite bead is used to connect the rest of the meter's ground to this ground plane then identical ferrite beads must be placed into the power supply lines (VDD and VSS) and into the current input lines from the shunt. If a single ferrite bead is placed some signals are filtered and others are not, which will create differential noise between the unfiltered and the filtered signals. This will affect the performance of the SA4104A in the presence of electromagnetic disturbance.

As far as the immunity to electromagnetic interference is concerned the guideline is simply to minimize the parasitic inductance. Each PCB net has a parasitic inductance and if this is not sufficiently small it could cause resonance with the parasitic capacitance at low enough frequencies to affect the performance on the HF interference test or the FTB test. Keeping the PCB tracks as short as possible is one method to avoid this scenario. Parasitic inductance is also a factor that can render the MOV almost useless because a voltage spike can be amplified in both magnitude and duration by series inductance. The capacitor in parallel with the MOV cancels some of this

inductance but still all measures to avoid parasitic inductance should be adhered to.

EXAMPLE DESIGNS

Example1

Nominal voltage: 220V
 Maximum current: 40A
 Basic current: 10A
 Shunt: 320 $\mu\Omega$; 12,5mV@ 40A
 Pulse constant: 1600imp/kWh
 Motor constant: 100imp/kWh

Using the design equations derived earlier:

equation(1): R18, R19, R20, R21=200 Ω
 equation(2): choose C11, C12, C13=100nF to obtain f_{-3dB} =15.9kHz which is adequate
 equation(4): R16=100 Ω
 equation(5): R17=10k Ω
 equation(8): R_x =200k Ω
 equation(9): choose R6=100k Ω and obtain R7=75k Ω
 equation(10): R8=20k Ω
 equation(11): R9 = 10k Ω , R10 = 4.7k Ω , R11 = 2.4k Ω , R12 = 1.2k Ω , R13 = 620 Ω , R14 = 300 Ω and R15 = 150 Ω . Some ratios are not entirely accurate, but to ensure low cost it is important to use only standard resistor values.
 equation(12): using IVP=11 obtain DF_LED=879
 equation(13): DF_MO=16
 Using Table 2 set FMS = '0', R3 = '1', R2 = '0', R1 = '1' and R0 = '0'.

Example 2

Nominal voltage: 220V
 Maximum current: 10A
 Basic current: 2.5A
 Shunt: 1m Ω ;10mV @ 10A
 Pulse constant: 3200imp/kWh
 Motor constant: 100imp/kWh

Using the design equations derived earlier:

equation(1): R18, R19, R20, R21 = 156 so set the value to 150 , the input current at I_{MAX} will be 16.7 μ A which is still sufficiently below the saturation point of the current inputs
 equation(2): choose C11, C12, C13=100nF to obtain f_{-3dB} =21.2 kHz which is still adequate
 equation(4): R16=75 Ω
 equation(5): R17=7.5k Ω
 The calibration network remains unchanged from example1.
 equation(12): using IVP=11 obtain DF_LED=1758
 equation(13): DF_MO=32
 Using Table 2 set FMS = '0', R3 = '0', R2 = '0', R1 = '1' and R0 = '1'.



RM4104ASEB

USING THE RM4104ASEB METER RM4104ASEB SETUP

The RM4104ASEB meter is equipped with several solderable selectors, which allow the meter to be set up according to the required specifications. Table 3 describes the functionality of the various jumpers. When working on the meter it should be noted that the meter is referenced to the live voltage and care should be taken to avoid electric shock.

Name	Option	Description
J1 to J8	Closed or Open	These jumpers are used for calibration purposes. Refer to the "Calibrating the Meter" section.
J9 to J11	Closed or Open	Closing these jumpers will connect the on-board power supply to the SA4104A and leaving them open will disconnect the on-board power supply from the SA4104A. This may be useful for debugging purposes.
J12 to J16	V _{DD} or V _{SS}	Used to select the required rated conditions. Refer to the "Setup of R0, R1, R2, R3 and FMS for Different Rated Conditions" section.

Table 3: RM4104ASEB Jumper options

EXTERNAL CONNECTIONS

The meter should be connected as shown in Table 4 and illustrated in Figure 5. The shunt is connected to J19, the Live In to J21 and the Neutral to J20. The external "+" and "-" terminals on the box are connected to the opto-isolator output, J22. The stepper motor is connected to J23.

Name	Function Description
1	LIVE IN: Live current input and Live voltage input if supplied separately
2	LIVE OUT: Live current output
3	No connection (Neutral output if required)
4	NEUTRAL: Neutral Voltage
+ and -	Opto-isolated pulse output. This should be connected to the measurement or calibration equipment if no optical pickup is available.

Table 4: External connection description

CALIBRATING THE METER

The RM4104ASEB is calibrated by means of a resistive ladder on the voltage sensing network. The eight resistors can be chosen to represent any desired calibration range. The calibration accuracy can be extended by adding resistors to the ladder network. Soldering a jumper in parallel with a resistor closed will remove that resistor from the voltage divider network thereby providing a higher input current to the SA4104A. The RM4104ASEB is calibrated by first short circuiting resistor R8. If the error is now positive a larger resistance is required so the jumper across R8 is opened before proceeding to the next resistor in the network (R9). If the error is negative then the process can be continued with the next resistor. These steps are repeated for all eight resistors in the ladder network. The SA4104A is linear over the dynamic range required by the IEC61036 specification, so calibration is only required at one current value. Typically the basic current (I_b) is chosen as the calibration point. The repeatability of error measurements at I_b is typically better than 0.1% so the error of the meter can be measured accurately by a single integration of a very small number of pulses.

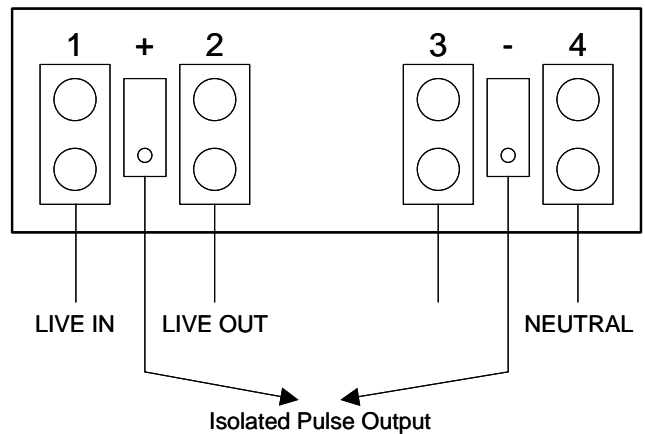


Figure 5: External connection diagram for the RM4104ASEB meter



METER SCHEMATICS

The circuit diagram shown below is a complete schematic of the RM4104ASEB meter based on the scenario of example 1 in the "Example Designs" section.

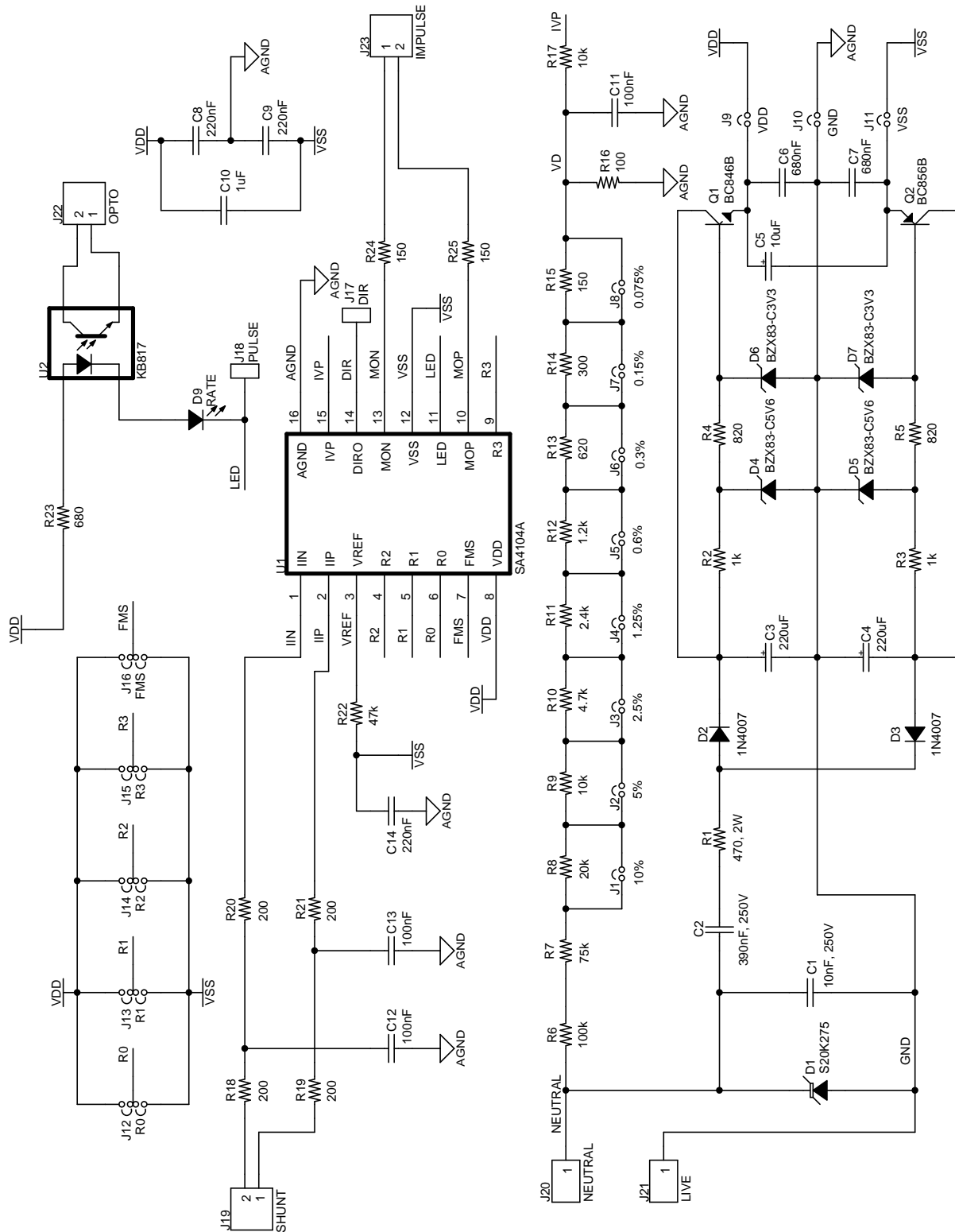


Figure 6: Complete RM4104ASEB meter schematic

**COMPONENT LIST**

The component list given in Table 5 below relates to the design example 1 of the “Example Designs” section.

Part	Detail	Description
C1	10nF, 250V, X2	Metallized polyester film capacitor, leaded
C2	390nF, 250V, X2	Polyester capacitor, leaded
C3, C4	220 μ F, 16V	Capacitor, electrolytic radial, leaded
C5	10 μ F, 16V	Capacitor, electrolytic radial, leaded
C6, C7	680nF	Capacitor, monolithic ceramic, SMD 0805
C8, C9, C14	220nF	Capacitor, monolithic ceramic, SMD 0805
C10	1 μ F	Capacitor, monolithic ceramic, SMD 0805
C11, C12, C13	100nF	Capacitor, monolithic ceramic, SMD 0805
R1	470 Ω	2W, 5%, wire-wound resistor, leaded
R2, R3	820 Ω	1/8W, 1%, metal film resistor, SMD 0805
R4, R5	1k Ω	1/8W, 1%, metal film resistor, SMD 0805
R6	100k Ω	1/8W, 1%, metal film resistor, SMD 0805
R7	75k Ω	1/8W, 1%, metal film resistor, SMD 0805
R8	20k Ω	1/8W, 1%, metal film resistor, SMD 0805
R9	10k Ω	1/8W, 1%, metal film resistor, SMD 0805
R10	4.7k Ω	1/8W, 1%, metal film resistor, SMD 0805
R11	2.4k Ω	1/8W, 1%, metal film resistor, SMD 0805
R12	1.2k Ω	1/8W, 1%, metal film resistor, SMD 0805
R13	620 Ω	1/8W, 1%, metal film resistor, SMD 0805
R14	300 Ω	1/8W, 1%, metal film resistor, SMD 0805
R15	150 Ω	1/8W, 1%, metal film resistor, SMD 0805
R16	100 Ω	1/8W, 1%, metal film resistor, SMD 0805
R17	10k Ω	1/8W, 1%, metal film resistor, SMD 0805
R18, R19, R20, R21	200 Ω	1/8W, 1%, metal film resistor, SMD 0805
R22	47k Ω	1/8W, 1%, metal film resistor, SMD 0805
R23	680 Ω	1/8W, 1%, metal film resistor, SMD 0805
R24, R25	150 Ω	1/8W, 1%, metal film resistor, SMD 0805
D1	S20K275	Metal oxide varistor
D2, D3	1N4007	Rectifier diode, leaded
D4, D5	BZX83-C5V6	5.6V zener diode, 5%, 0.5W, leaded
D6, D7	BZX83-C3V3	3.3V zener diode, 5%, 0.5W, leaded
D9	LED	3mm, RED
Q1	BC846B	NPN transistor, SMD SOT23
Q2	BC856B	PNP transistor, SMD SOT23
U1	SA4104A	Energy meter device, 16-pin SOIC, 0.8mm
U2	KB817	Opto-isolator, 4-pin PDIP, 2.54mm

Table 5: Component list for the RM4104ASEB meter



TYPICAL PERFORMANCE CURVES

The following performance curves show typical results obtained with several RM4104ASEB meters based on example 1 in the "Example Designs" section.

RM4104ASEB Performance at UPF for a 220V, 10(40)A Meter

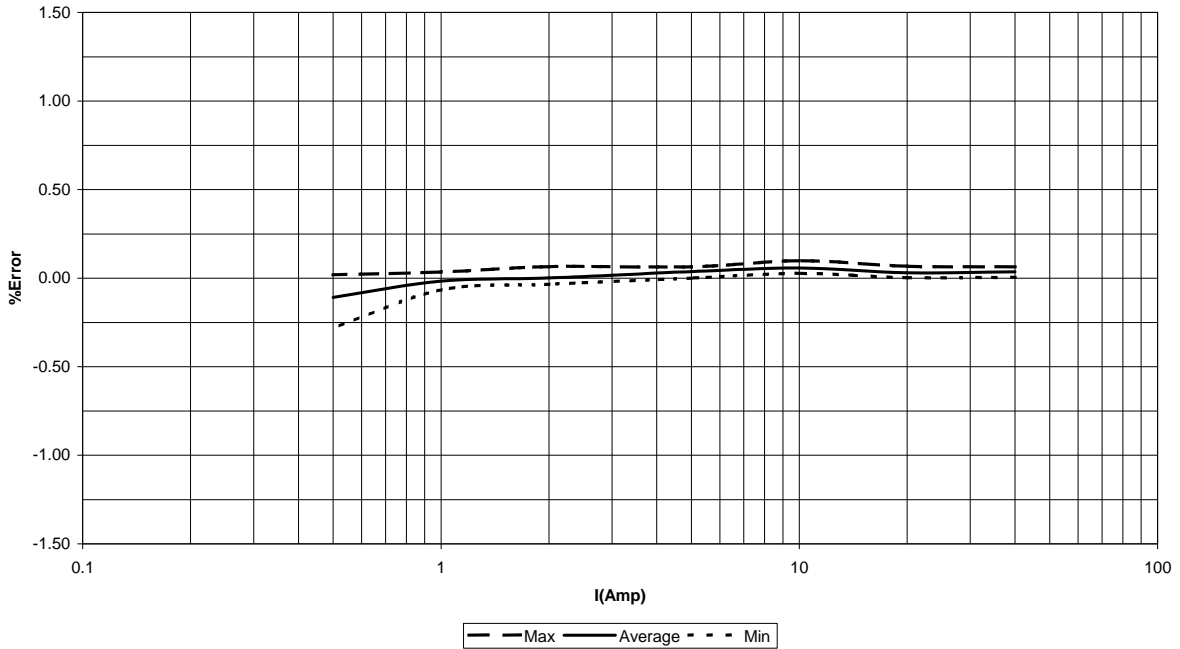


Figure 7: Typical performance of the RM4104ASEB at unity power factor

RM4104ASEB Performance at 0.5LAG for a 220V, 10(40)A Meter

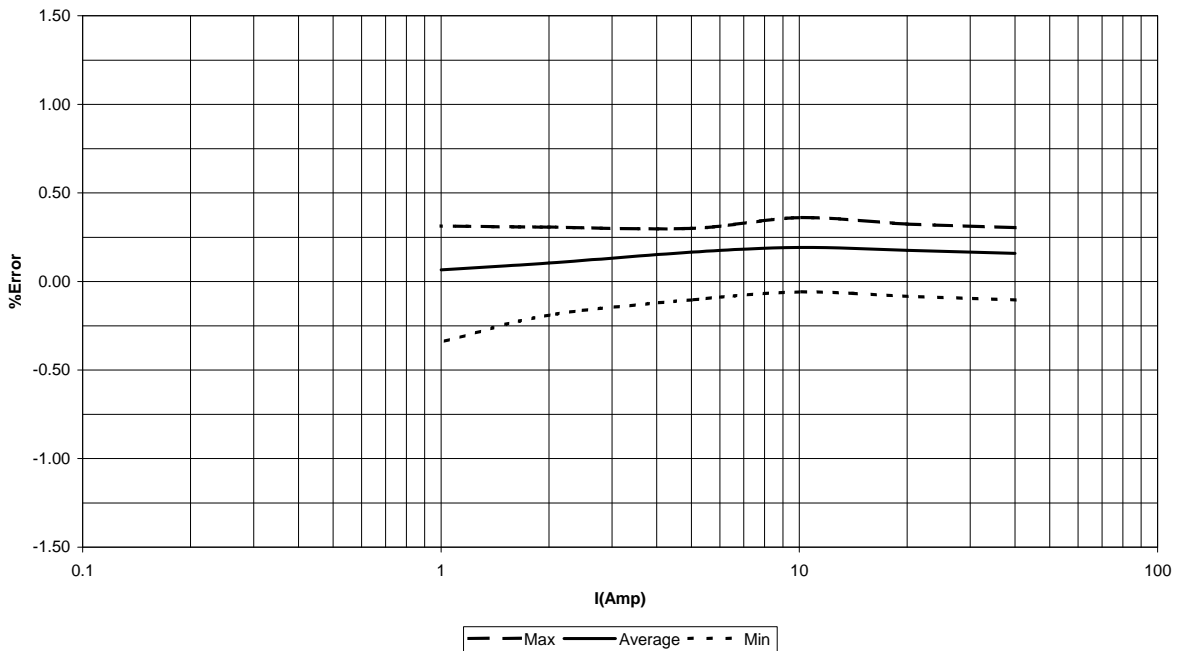


Figure 8: Typical performance of the RM4104ASEB at 0.5 lag power factor

RM4104ASEB Performance at 0.8LEAD for a 220V, 10(40)A Meter

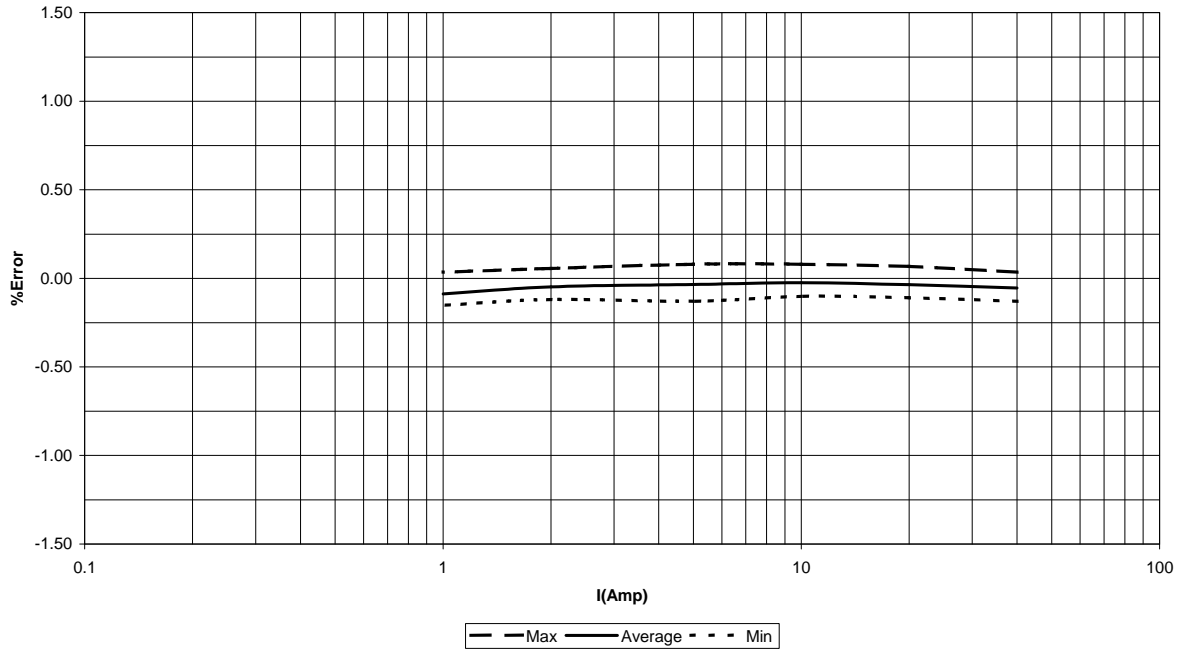


Figure 9: Typical performance of the RM4104ASEB at 0.8 lead power factor



PCB LAYOUT

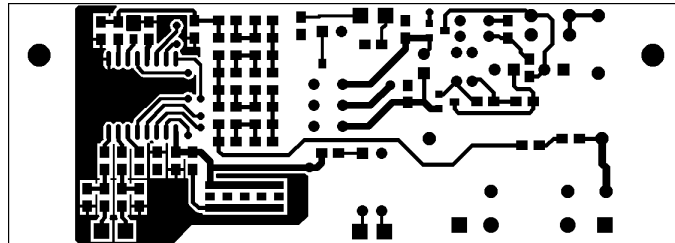


Figure 10: PCB Top Layer (Scale 1:1)

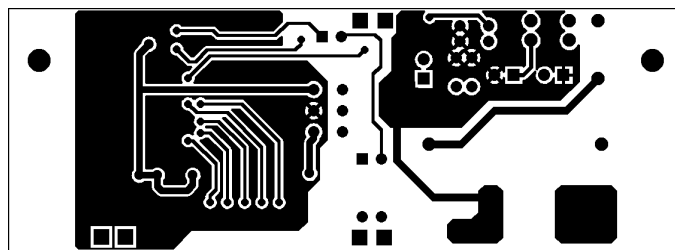


Figure 11: PCB Bottom Layer (Scale 1:1)

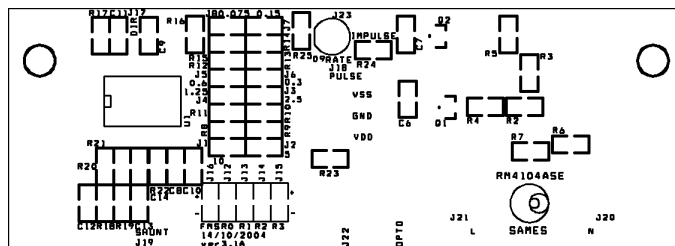


Figure 12: PCB Silkscreen Top Layer (Scale 1:1)

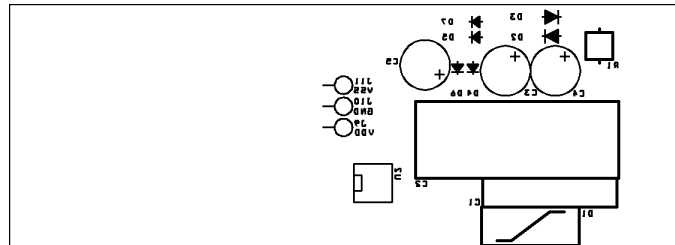


Figure 13: PCB Silkscreen Bottom Layer (Scale 1:1)

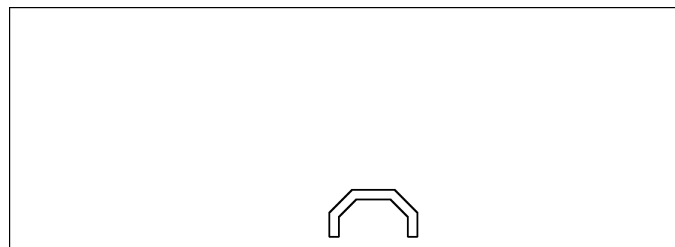


Figure 14: PCB Mechanical Layer (Scale 1:1)

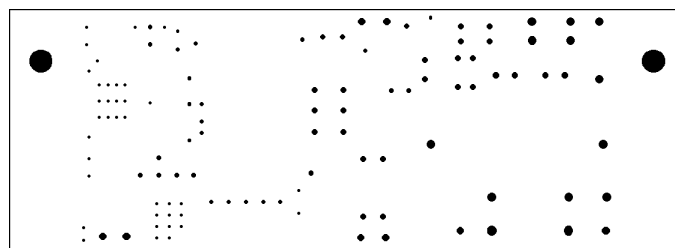


Figure 15: PCB Drill Drawing Top/Bottom Layer (Scale 1:1)



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NOTES



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