Multifunction Three Phase Energy Metering IC with SPI Interface

SA5301A

ICDC

FEATURES

- Bidirectional active and reactive energy measurement
- Voltage and current RMS measurement
- Mains frequency and phase angle measurement
- SPI communication interface with optional CRC
- Accuracy is compliant with IEC 62053-21, IEC 62053-22 and IEC 62053-23 standards
- Configurable active and reactive pulse output module
- Configurable status and error conditions
- Four configurable output pins
- Operates over a wide range of temperatures and power supply voltages
- Precision on-chip voltage reference and oscillator

DESCRIPTION

The SA5301A is a high accuracy three phase bidirectional energy/power metering integrated circuit. It has been designed to measure various additional quantities over and above active energy. This makes it an ideal device for use in multi-function three phase energy meters for residential or industrial purposes, as well as energy monitoring and control applications.

The SA5301A is capable of measuring active and reactive energy on a per channel basis to an accuracy of less than 0.1 % error over a 1000:1 current range. True RMS voltage and current, as well as mains frequency and phase angle, are also measured. Data is accessible via an integrated SPI serial interface. The device includes a fully programmable pulse output module to automatically generate active and reactive energy pulses. A multitude of programmable status and interrupt conditions can be configured to assist in monitoring various aspects pertaining to energy consumption. Four configurable output pins allow various status signals to be monitored directly.

The SA5301A includes a precision oscillator and voltage reference to ensure the circuitry maintains stable operation over a wide temperature and power supply range. Very few other external components are required.

The SA5301A integrated circuit is available in a 24 pin small outline (SOIC24) RoHS compliant package.

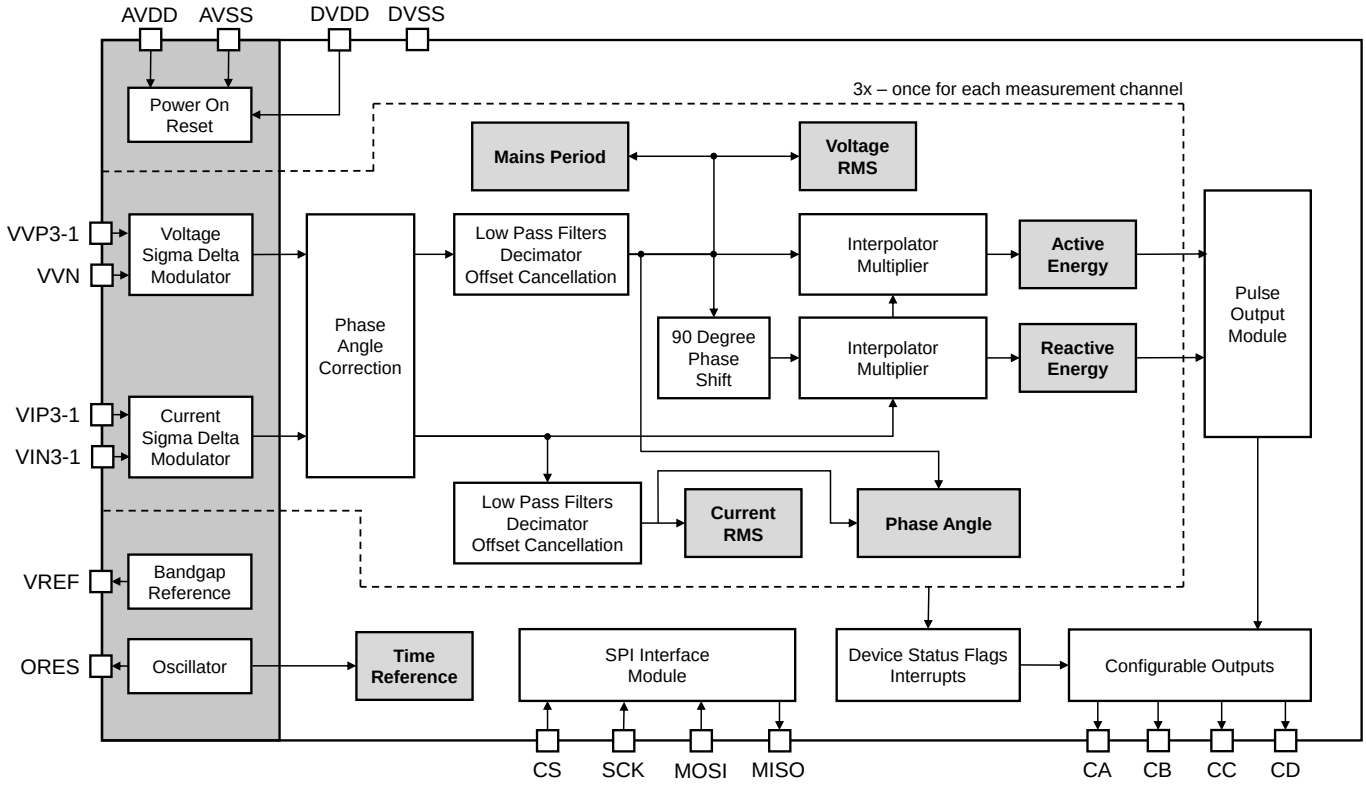


Figure 1: *SA5301A block diagram*

ELECTRICAL SPECIFICATIONS

AV_{DD} = 5 V ±10 %, DV_{DD} = 3.3 V ±10 %, over the temperature range −40 °C to 85 °C, unless otherwise specified. All configuration registers contain their default settings. Refer to Figure 2 for test circuit.

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Supplies						
Supply Voltage: Analog	AV_{DD}	4.5	5.0	5.5	V	
Supply Voltage: Digital	DV_{DD}	2.5	3.3	5.5	V	
Supply Current: Analog	AI_{DD}	2.5	3.0	3.6	mA	
Supply Current: Digital	DI_{DD}	1.5	2.2	6.0	mA	
Analog Inputs						
Current Signal Inputs (Differential)						
Input Voltage Range	IVR_I	−300		300	mV	
Differential Input Voltage Range	$DIVR_I$	−300		300	mV	
Common Mode Input Voltage Range	$CIVR_I$	−150		150	mV	
Input Leakage	IL_I	−3		1	µA	
Input Impedance (Differential)	ZID_I	54	60	66	kΩ	
Offset Voltage (Input Referred)	VO_I	−10		10	mV	
Voltage Signal Inputs (Single-Ended)						
Input Voltage Range	IVR_V	−300		300	mV	
Input Leakage	IL_V	−3		1	µA	
Input Impedance	ZI_V	54	60	66	kΩ	
Offset Voltage (Input Referred)	VO_V	−10		10	mV	
On-chip Voltage Reference						
Reference Voltage	V_R	1.20	1.225	1.25	V	
Temperature Coefficient	$\lvert TC_R \rvert$		10	25	ppm/°C	
On-chip Oscillator						
Oscillator Frequency	f_{OSC}	1.70	1.786	1.875	MHz	when using a 100 kΩ resistor on ORES
Temperature Coefficient	$\lvert TC_{OSC} \rvert$		10	25	ppm/°C	excluding temperature coefficient of external resistor
Digital Inputs (CS, SCK, MOSI, MISO floating)						
Input High Voltage	V_{IH}	75 % DV_{DD}			V	
Input Low Voltage	V_{IL}			25 % DV_{DD}	V	
Input Leakage	I_L	−1		1	µA	
Input Capacitance	C_I			10	pF	
Digital Outputs (MISO, CA, CB, CC, CD)						
Output High Voltage	V_{OH}	DV_{DD}−0.8			V	I_{SOURCE} = 5 mA
Output Low Voltage	V_{OL}			0.5	V	I_{SINK} = 5 mA

ENERGY MEASUREMENT SPECIFICATIONS

AV_{DD} = 5 V ±10 %, DV_{DD} = 3.3 V ±10 %, over the temperature range −40 °C to 85 °C, unless otherwise specified. All configuration registers contain their default settings. Refer to Figure 2 for test circuit.

Parameter	Symbol	Min	Typ	Max	Unit	Condition
General						
Mains Frequency Range	f_{MAINS}	30	50 or 60	100	Hz	
Phase Angle Correction	ph_{CORR}	−2.57		2.57	°	at 50 Hz in 255 steps of approx. 0.01°
Active Energy						
Register Pulse Rate	$f_{REG-ACT}$	180	190	200	kHz	200 mV_{RMS} input signals
Pulse Output Pulse Rate	$f_{OUT-ACT}$	4.75	5.0	5.25	kHz	200 mV_{RMS} input signals, default settings
Linearity Error	Err_{ACT}	−0.1		0.1	%	|PF| > 0.5, dynamic range 1000:1
Temperature Coefficient	$\|TC_{ACT}\|$		30	100	ppm/°C	
Reactive Energy						
Register Pulse Rate	$f_{REG-RCT}$	180	190	200	kHz	200 mV_{RMS} input signals
Pulse Output Pulse Rate	$f_{OUT-RCT}$	4.25	5.0	5.75	kHz	200 mV_{RMS} input signals, default settings
Linearity Error	Err_{RCT}	−0.1		0.1	%	|PF| < 0.8, dynamic range 1000:1
Temperature Coefficient	$\|TC_{RCT}\|$		30	100	ppm/°C	
Voltage and Current RMS						
Voltage RMS Error	Err_{VRMS}	−0.5		0.5	%	voltage dynamic range 50:1
Current RMS Error	Err_{IRMS}	−0.5		0.5	%	current dynamic range 1000:1
Settling Time	ts_{RMS}		16		Mains cycles	to 99 % of final value

ABSOLUTE MAXIMUM RATINGS

Exposure to stresses exceeding the “Absolute Maximum Ratings” may cause permanent damage to the device or affect device reliability. The functional operation and specifications of the device are only guaranteed if all parameters are kept within the normal operating conditions.

Parameter	Symbol	Min	Max	Unit
Supply Voltage	AV_{DD} / DV_{DD}	−0.3	6	V
Voltage on any Pin	V_{PIN}	−0.5	Supply voltage +0.5 V	V
Current on any Pin	I_{PIN}	−150	150	mA
Storage Temperature	T_{STG}	−60	125	°C
Specified Operating Temperature Range	T_O	−40	85	°C
Limit Range of Operating Temperature	T_{limit}	−50	100	°C

During manufacturing, testing and shipment great care is taken to protect the devices against potential external environmental damage such as electrostatic discharge (ESD). Although the device includes ESD protection circuitry, permanent damage may occur if it is subjected to high-energy electrostatic discharges accumulated on the human body or test equipment that can discharge without detection. Therefore, proper ESD precautions are recommended during device handling to avoid performance degradation, loss of functionality or reliability issues.

ATTENTION: Electrostatic sensitive device. Requires special handling.

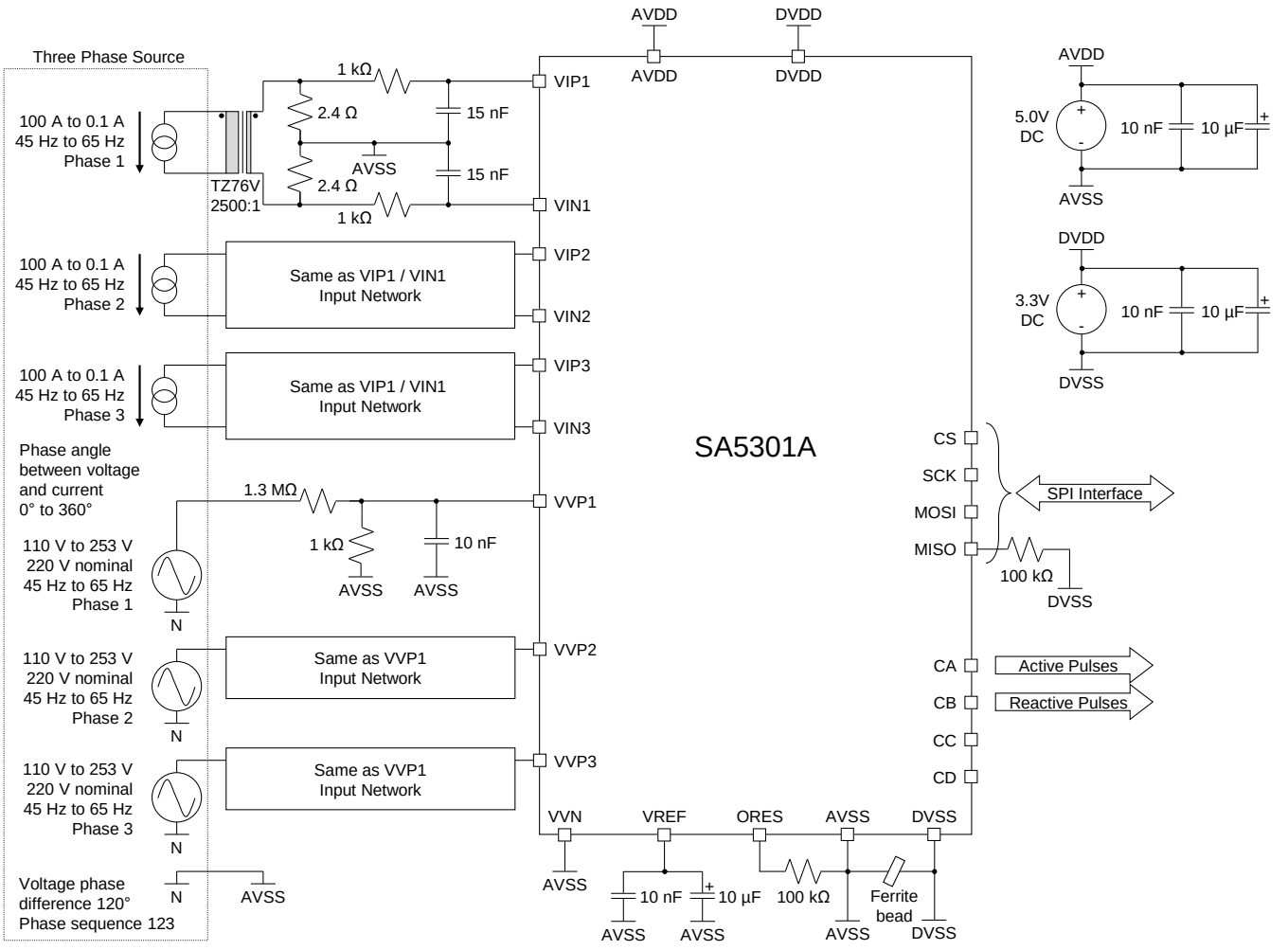
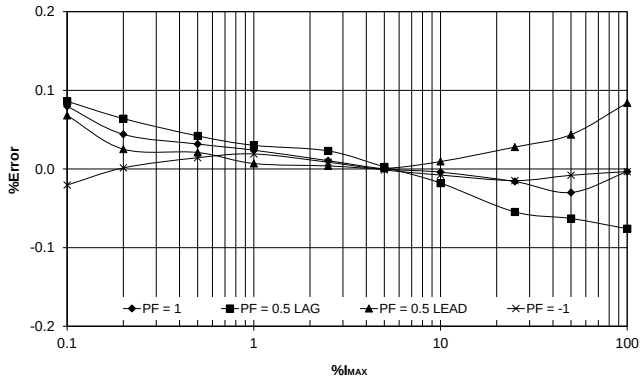


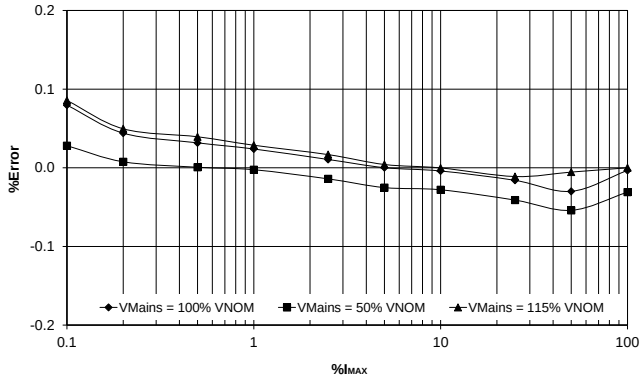
Figure 2: *Test circuit for electrical characteristics*

PERFORMANCE GRAPHS

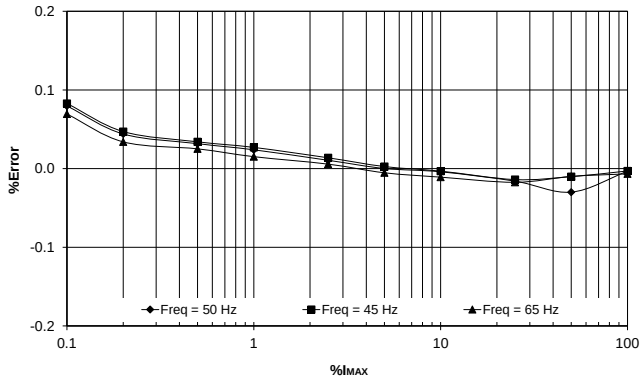
AV_{DD} = 5 V ±10 %, DV_{DD} = 3.3 V ±10 %, over the temperature range −40 °C to 85 °C, unless otherwise specified. All configuration registers contain their default settings. Refer to Figure 2 for test circuit.



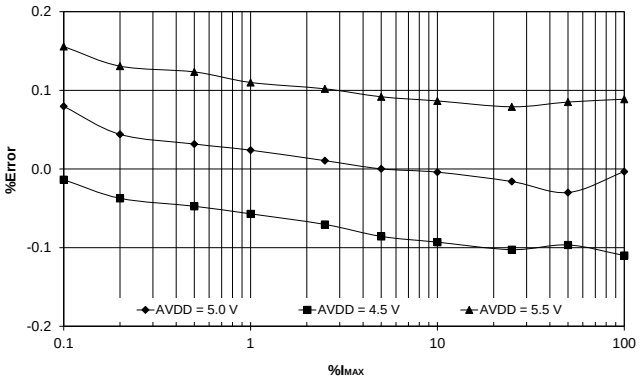
Graph 1: *Active energy load linearity with power factor, Balanced 3 phase, Freq = 50 Hz, VMains = V_{NOM}, Temp = 25 °C, AV_{DD} = 5.0 V*



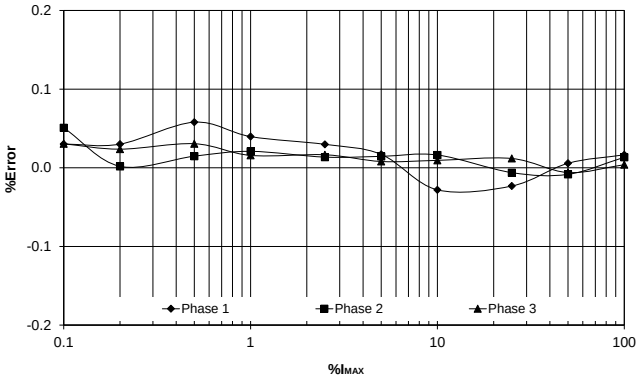
Graph 2: *Active energy load linearity with mains voltage, Balanced 3 phase, PF = 1, Freq = 50 Hz, Temp = 25 °C, AV_{DD} = 5.0 V*



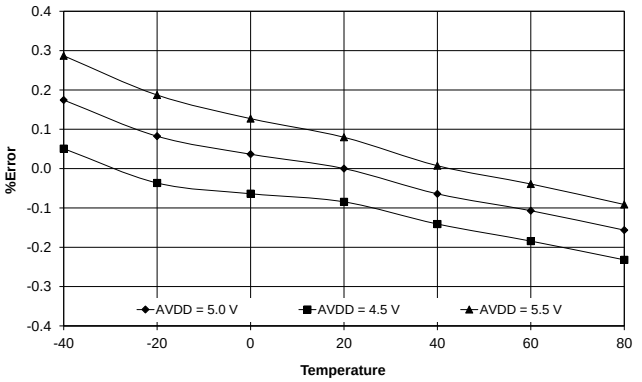
Graph 3: *Active energy load linearity with frequency, Balanced 3 phase, PF = 1, VMains = V_{NOM}, Temp = 25 °C, AV_{DD} = 5.0 V*



Graph 4: *Active energy load linearity with AV_{DD}, Balanced 3 phase, PF = 1, Freq = 50 Hz, VMains = V_{NOM}, Temp = 25 °C*

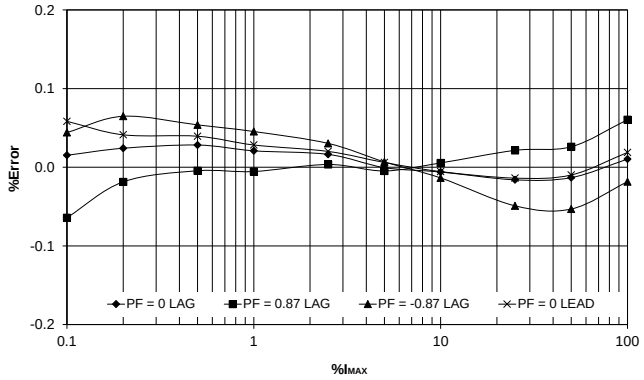


Graph 5: *Active energy load linearity for 3 voltage 1 current, all phases, PF = 1, Freq = 50 Hz, VMains = V_{NOM}, Temp = 25 °C, AV_{DD} = 5.0 V*

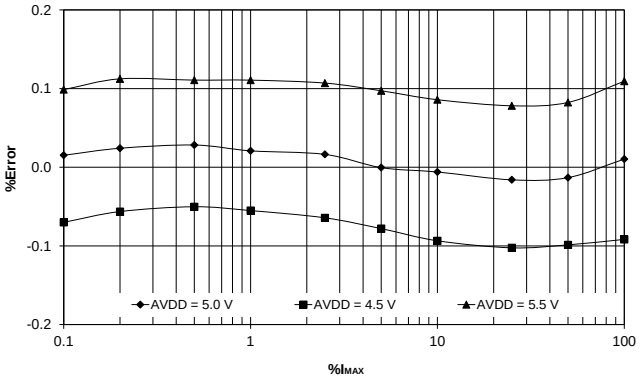


Graph 6: *Active energy gain vs. temperature with AV_{DD}, Balanced 3 phase, PF = 1, Freq = 50 Hz, VMains = V_{NOM}, IMains = 25 % I_{MAX}*

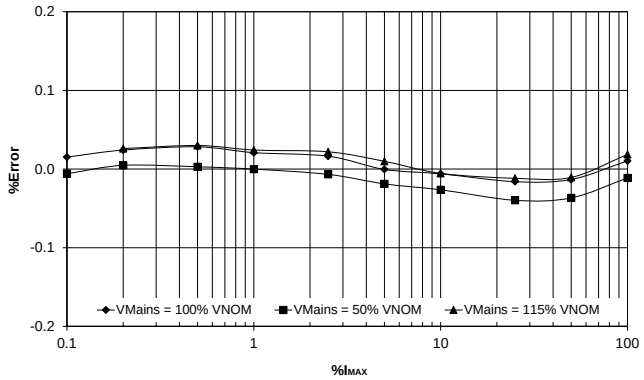
AV_{DD} = 5 V ±10 %, DV_{DD} = 3.3 V ±10 %, over the temperature range −40 °C to 85 °C, unless otherwise specified. All configuration registers contain their default settings. Refer to Figure 2 for test circuit.



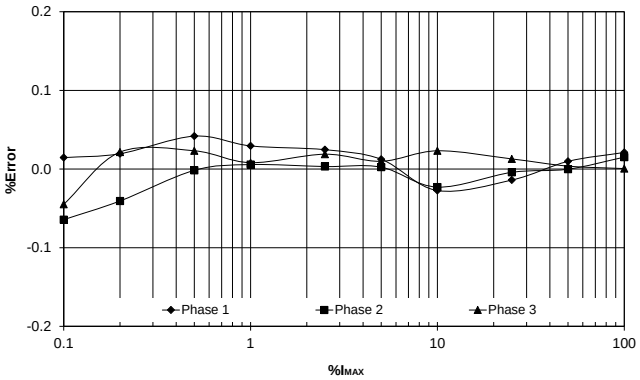
Graph 7: *Reactive energy load linearity with power factor, Balanced 3 phase, Freq = 50 Hz, VMains = V_{NOM}, Temp = 25 °C, AV_{DD} = 5.0 V*



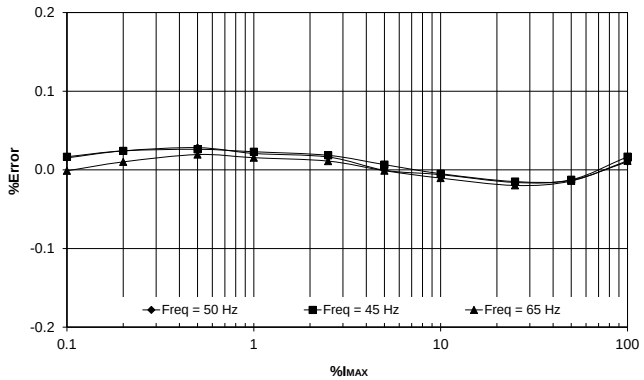
Graph 10: *Reactive energy load linearity with AV_{DD}, Balanced 3 phase, PF = 0, Freq = 50 Hz, VMains = V_{NOM}, Temp = 25 °C*



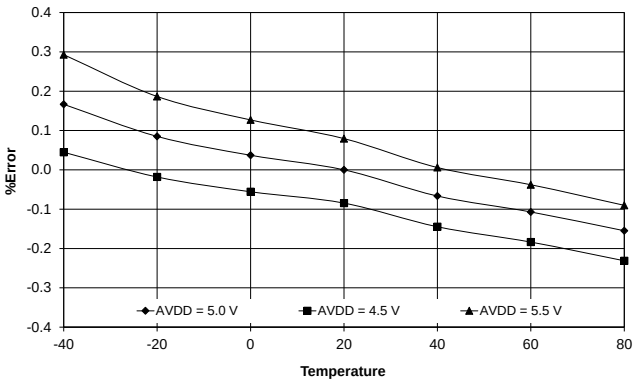
Graph 8: *Reactive energy load linearity with mains voltage, Balanced 3 phase, PF = 0, Freq = 50 Hz, Temp = 25 °C, AV_{DD} = 5.0 V*



Graph 11: *Reactive energy load linearity for 3 voltage 1 current, all phases, PF = 0, Freq = 50 Hz, VMains = V_{NOM}, Temp = 25 °C, AV_{DD} = 5.0 V*



Graph 9: *Reactive energy load linearity with frequency, Balanced 3 phase, PF = 0, VMains = V_{NOM}, Temp = 25 °C, AV_{DD} = 5.0 V*



Graph 12: *Reactive energy gain vs. temperature with AV_{DD}, Balanced 3 phase, PF = 0, Freq = 50 Hz, VMains = V_{NOM}, IMains = 25 % I_{MAX}*

PIN DESCRIPTION

Designation	Pin No.	Description
AVSS	7	Analog supply ground - connect this to the analog system ground.
AVDD	18	Supply voltage for analog circuits - should be between 4.5 V and 5.5 V (5.0 V nominal) for specified performance. A 10 µF with 10 nF capacitor decoupling network is required to the analog system ground.
DVSS	8	Digital supply ground - connect this to the digital system ground. The analog and digital system grounds should be connected together at one point only.
DVDD	17	Supply voltage for digital circuits - should be between 2.5 V and 5.5 V (2.5 V, 3.3 V or 5.0 V nominal). A 10 µF with 10 nF capacitor decoupling network is required to the digital system ground.
VREF	5	Reference voltage output - this pin must be decoupled to the analog system ground via a 10 µF with 10 nF capacitor decoupling network.
ORES	6	Oscillator reference resistor - this pin must be connected to the analog system ground via a resistor with a nominal value of 100 kΩ. Since the oscillator stability depends on this resistor a high stability resistor is recommended. No external capacitance should be added.
VVP1 VVP2 VVP3	3 2 1	Mains voltage signal inputs - these inputs measure the mains voltage signals for the three phases. Signals representing the mains voltages with a maximum peak amplitude of 300 mV to VVN are required. Anti-alias filters should be incorporated in the mains voltage scaling networks for optimum performance.
VVN	4	Mains neutral signal input - this pin must be connected directly to the mains neutral signal level, which is typically also the analog system ground. An anti-alias filter must not be used, to prevent cross coupling between voltage channels.
VIP1, VIN1 VIP2, VIN2 VIP3, VIN3	19, 20 21, 22 23, 24	Current signal inputs - these differential inputs measure the line current signals for the three phases. Signals representing the line currents with a maximum differential peak amplitude of 300 mV are required. Anti-alias filters should be incorporated in the current scaling networks for optimum performance. The common mode level of these signals should be limited to 150 mV to avoid high leakage currents on the input pins and prevent device latch-up.
CS SCK MOSI MISO	16 15 14 13	SPI interface - these pins form the SPI interface to the device. CS is the active high chip select, SCK is the clock input, MOSI is the data input and MISO is the data output line. The device samples MOSI and writes data on MISO on the rising edge of SCK when CS is high. MISO is floating unless data is being read from the device.
CA	9	Configurable output pin A - can be configured to output any of the configurable output signals, the default is the active pulse output from the pulse output module.
CB	10	Configurable output pin B - can be configured to output any of the configurable output signals, the default is the reactive pulse output from the pulse output module.
CC	11	Configurable output pin C - can be configured to output any of the configurable output signals, the default is the mains voltage crossover pulses from all three phases.
CD	12	Configurable output Pin D - can be configured to output any of the configurable output signals, the default is the interrupt signal that indicates that a configured interrupt condition has occurred.

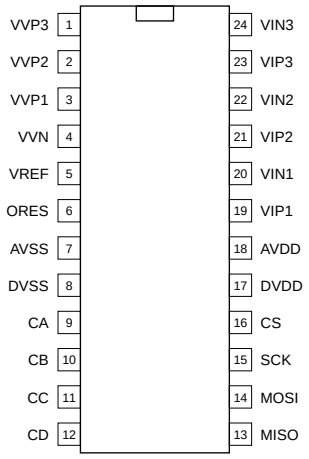


Figure 3: *Pin connections*

ORDERING INFORMATION

Part Number	Package
SA5301ASAR	SOIC24 (RoHS compliant)

SA5301A ARCHITECTURE

The SA5301A is a CMOS mixed-signal integrated circuit that performs various multifunction power and energy metering calculations. It is a combination of three identical measurement channels, one for each of the three energy measurement phases, combined with some common circuitry. For the most part the three channels operate independently of one another. A range of writeable and readable registers are accessible via the SPI interface. This serves as the primary method of setting up the device and retrieving the measurement data.

The following sections describe each of the building blocks of the SA5301A in detail. Refer to Figure 1 for an overview and illustration of how the building blocks are interlinked.

REGISTER MAP

The registers, which are accessible via the SPI interface, are arranged in 4 banks. Each bank has 64 unique register addresses, but not all are used. Bank 0 is for common settings and data, while banks 1 to 3 are for each respective measurement channel of the device. Banks 1 to 3 contain an identical set of registers. There are four types of registers:

- W16: 16-bit writeable register used to capture configuration information
- R16: 16-bit readable register used to access status and measurement data
- R24: 24-bit readable register used to access measurement data
- R24-C: 24-bit readable register used to access measurement data, with an optional clear feature, which can automatically clear the register after each read.

Registers can be read in either 16-bit or 24-bit mode. When reading a 16-bit register in 24-bit mode the register will be padded with 8 zeros before the most significant bit. When reading a 24-bit register in 16-bit mode the 8 least significant bits will be truncated.

Table 1: *SA5301A register map*

Bank	Address		Type	Description
0	000000	0x00	R16	Global status register
0	011111	0x1f	R24-C	Time reference register
0	100001	0x21	W16	Active pulse output divider register
0	100010	0x22	W16	Reactive pulse output divider register
0	100011	0x23	W16	Pulse output setup register
0	111110	0x3e	W16	Configurable outputs setup register
0	111111	0x3f	W16	Status and interrupt setup register
1-3	000000	0x00	R16	Bank status register for the specific measurement channel
1-3	000001	0x01	R24-C	Active energy register for the specific measurement channel
1-3	000010	0x02	R24-C	Reactive energy register for the specific measurement channel
1-3	000011	0x03	R24	Voltage RMS register for the specific measurement channel
1-3	000100	0x04	R24	Current RMS register for the specific measurement channel
1-3	000101	0x05	R16	Mains period register for the specific measurement channel
1-3	000110	0x06	R16	Phase angle register for the specific measurement channel
1-3	100000	0x20	W16	Pulse output calibration register for the specific measurement channel
1-3	111001	0x39	W16	Channel performance tuning register for the specific measurement channel
1-3	111010	0x3a	W16	Channel settings register for the specific measurement channel
1-3	111011	0x3b	W16	Phase shift correction register for the specific measurement channel
1-3	111100	0x3c	W16	Voltage status parameters register for the specific measurement channel
1-3	111101	0x3d	W16	Current status parameters register for the specific measurement channel

TYPICAL METER ARCHITECTURE

Figure 4 shows the typical meter architecture for an energy meter based on the SA5301A. A micro-controller is used in conjunction with the SA5301A to implement the various features required for a multi-function meter. The SA5301A supplies all the relevant data regarding energy consumption to the controller for further processing. The voltage and current sensing networks translate the mains voltages and mains currents to signals that can be further processed by the SA5301A.

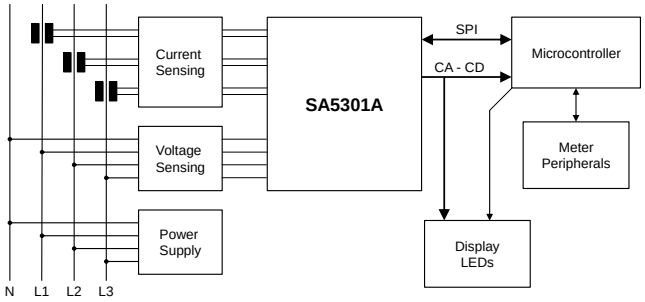


Figure 4: *Typical meter configuration for an SA5301A based energy meter*

POWER SUPPLIES

The SA5301A has split power supplies for the analog and digital circuits. This allows the analog circuits to be isolated from the typical noise present on digital power supplies. Additionally a wider range of digital IO voltages can be accommodated. The analog circuits require a 5 V ±10 % supply to operate. The digital circuits can operate on any supply voltage between 2.5 V and 5 V nominal. The digital supply voltage determines the signalling level of the digital input and output pins.

Both supplies need to be adequately bypassed to their respective ground pins. A 10 µF tantalum electrolytic capacitor in parallel with a 10 nF ceramic capacitor is recommended.

Power Consumption

Analog power consumption is typically in the order of 15 mW. Digital power consumption is highly dependent on the digital supply voltage used and increases substantially as the supply voltage increases. In order to keep overall power consumption as low as possible it is recommended not to exceed a DV_{DD} of 3.3 V. In this case digital power consumption is 7.25 mW nominal.

Power-On Reset Circuit

The power-on reset circuit monitors both the analog and digital supply voltages and holds the device in reset until the analog supply voltage exceeds 4 V and the digital supply voltage exceeds 2.5 V. The global status register has a flag bit that indicates if a reset has occurred.

BANDGAP VOLTAGE REFERENCE

The bandgap voltage reference generates a stable 1.225 V (typical) reference voltage for the integrated oscillator and the sigma-delta converters. External capacitance needs to be added to the reference voltage node in order to filter transients and noise. This is done by adding a recommended 10 µF tantalum capacitor in parallel with a 10 nF ceramic capacitor on the VREF pin. Capacitors with a fairly low ESR are recommended. The bandgap reference achieves a typical temperature coefficient of 10 ppm/°C.

OSCILLATOR

The oscillator generates a clock signal for the device at a nominal frequency of 1.786 MHz (nominal clock period 560 ns). The frequency is determined by an external resistor attached to the ORES pin with a recommended value of 100 kΩ to achieve the nominal oscillator frequency. No external capacitance should be connected to the ORES pin as this will introduce jitter on the oscillator and degrade device performance.

The oscillator frequency is inversely proportional to the external resistor value. In order to reduce oscillator noise and improve temperature stability, a metal film resistor is required. This resistor can be used to null the temperature coefficient of other external circuits if required, refer to the Temperature Compensation section. The oscillator achieves a typical temperature coefficient of 10 ppm/°C, excluding any effects introduced by the external resistor.

SIGMA-DELTA MODULATORS

Each of the three measurement channels of the SA5301A contains two analog to digital converters based on 2nd order sigma-delta modulators. One is used for measuring a signal representing the mains voltage, the other for the line current. The modulators for the voltage signals accept single-ended input signals, their negative signal inputs are all connected together on the VVN pin. The modulators used for the current signals require differential signal inputs. All modulators saturate at an input signal amplitude of one quarter the bandgap reference voltage, i.e. 306 mV. The absolute signal level on a modulator input (VVP3-VVP1, VVN, VIP3-VIP1, VIN3-VIN1) must not exceed a level of 350 mV below the level of AVSS. This will lead to a drastic reduction in input impedance on that pin and could lead to device latch-up.

To allow for bandgap reference voltage variations, offsets and possible non-linearities close to the saturation limit, the maximum nominal input signal to the modulators has been defined as 200 mV_{RMS} (283 mV_{PEAK}). This maintains sufficient headroom before saturation occurs, and good performance should be guaranteed up to 300 mV_{PEAK}, which is defined as the full-scale input signal.

Current Sensing Network

Figure 5 shows the current sensing network for one measurement channel, and needs to be repeated for the two remaining channels. The resistor values should be selected to provide the SA5301A with a 200 mV_{RMS} differential input signal at maximum rated mains current, I_{MAX}.

The SA5301A requires the use of current transformers to provide electrical isolation to the line voltages when sensing the currents. The resistors R_1 and R_2 together form the termination resistor for the current transformer. The reference level is connected in the centre of the termination resistor to achieve a purely differential input signal. The ground reference level of the current sensing network should be the analog system ground of the meter, which is connected to AVSS of the SA5301A.

$$R_1 = R_2 = \frac{200\,\text{mV}}{2I_{\text{MAX}}/N}$$

where
I_{MAX} is the maximum rated mains current of the meter and
N is the turns ratio of the current transformer.

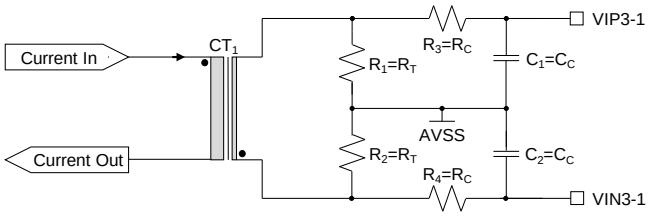


Figure 5: *Current sensing network*

For optimal performance the SA5301A requires anti-alias filters on the current signal inputs. These filters are realized by means of the capacitors C_1 and C_2 together with the resistors R_3 and R_4. The typical cut-off frequency of these filters should be between 10 kHz and 20 kHz. The resistor values of R_3 and R_4 must be equal and large enough to ensure reasonably sized capacitors. Additionally, the resistor value should not be too large to limit significant interaction with the modulator input impedance. For most scenarios an optimum input network is achieved by setting R_3 and R_4 to 1 kΩ and C_1 and C_2 to 15 nF. The anti-alias filter cut-off frequency, f_{CC}, is then 10.6 kHz. The total phase shift of the current sensing network, ϕ_C, can be calculated as the sum of the phase shift of the anti-alias filter and the phase shift of the current transformer.

$$f_{\text{CC}} = \frac{1}{2\pi R_{\text{C}} C_{\text{C}}}$$

$$\phi_{\text{C}} = -\arctan\left(2\pi R_{\text{C}} C_{\text{C}} \times f_{\text{MAINS}}\right) + \phi_{\text{CT}}$$

where
f_{MAINS} is the mains frequency of the meter and
ϕ_{CT} is the phase shift of the current transformer.

Voltage Sensing Network

Figure 6 shows the voltage sensing network for one measurement channel, and needs to be repeated for the two remaining channels. This circuit attenuates the mains voltage signal to the level required by the SA5301A. The attenuation ratio should be designed so that the input signal to the SA5301A is 200 mV_{RMS} at the maximum mains voltage (V_{MAX}) that the meter must be able to operate at. V_{MAX} is typically 15 % to 30 % larger than the nominal mains voltage (V_{NOM}) of the meter. The ground reference level of the voltage sensing network should be the analog system ground of the meter, which is connected to AVSS of the SA5301A. The VVN pin is the reference level for the voltage signal inputs and should also be directly connected to the analog system ground.

The resistor R_1 defines the output resistance of the voltage sensing network. It should not be too small, else the capacitor value will be quite large. However, if it is too large, inaccuracies will occur in the interaction with the input impedance of the SA5301A voltage signal input. An optimum input network is achieved by setting R_1 to 1 kΩ. R_2 is typically split into multiple similarly sized resistors, in order to limit the power dissipation and voltage across each resistor.

$$R_2 = \left(\frac{V_{\text{MAX}}}{200\,\text{mV}} \times R_1\right) - R_1$$

where
V_{MAX} is the maximum mains voltage the meter needs to operate at.

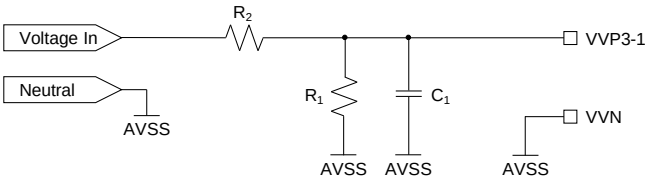


Figure 6: *Voltage sensing network*

For optimal performance the SA5301A requires an anti-alias filter on the voltage signal inputs. Referring to Figure 6, the capacitor C_1 is used to both implement the anti-alias filter and compensate for any phase shift caused by the current transformer on the current sensing network. Even though the SA5301A contains a phase shift error compensation feature, it is still recommended to compensate the phase angle difference between the voltage and current networks externally. Fine tuning the compensation can then be done using the SA5301A phase shift compensation feature. The cut-off frequency of the anti-alias filter is adjusted so that the phase shift of the voltage sensing network is identical to the sum of the phase shifts of the current transformer and the current sensing network anti-alias filter.

The value of the voltage sensing network capacitor and the anti-alias filter cut-off frequency may be determined using:

$$\phi_V = \phi_C$$

$$C_1 = \frac{|\tan \phi_V|}{2\pi R_1 \times f_{MAINS}}$$

$$f_{CV} = \frac{1}{2\pi R_1 C_1}$$

where
f_{MAINS} is the mains frequency of the meter and
ϕ_C is the phase shift of the current sensing network.

The effect of the current transformer phase shift is an increase in cut-off frequency of the the anti-alias filter on the voltage sensing network. A cut-off frequency up to 25 kHz is usually acceptable due to the smaller dynamic range of the mains voltage signal. For example, a good quality current transformer might have a phase shift of 0.09° resulting in a C_1 of 10 nF and a cut-off frequency of 16 kHz. No anti-alias filter should be used on the VVN input pin, it will cause cross-coupling between voltage channels if the mains voltages are unbalanced.

PHASE SHIFT CORRECTION

The external anti-alias filters and current transformers will always add a phase shift to the voltage and current input signals. As long as the phase shifts on the voltage and current paths are exactly equal, energy measurement accuracy is not affected. It is virtually impossible to compensate unequal phase shifts externally to ensure negligible energy measurement error. The SA5301A includes phase shift correction circuitry, that allows the phase shifts of the voltage and current input signals to be equalised. The phase shift correction circuit operates on the output signals from the modulators, before any further processing is performed. The phase shift correction registers (banks 1-3, address 0x3b) control the amount of phase correction applied.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								P8	P7	P6	P5	P4	P3	P2	P1	P0
Default								0	0	0	0	0	0	0	0	0

Figure 7: *Phase shift correction register*

This register contains 9 bits that control the phase shift correction circuit. Each measurement channel of the SA5301A has a programmable delay circuit that can adjust the delay between the voltage and current signals in order to correct for phase shift differences in the current and voltage sensing networks. The correction is based on a simple time delay of one of the two signals, depending on whether a positive or negative phase shift correction is required. It is still recommended that rough correction be performed externally, by varying the cut-off frequency of the external anti-alias filters. The on-chip correction feature can then be used to correct for component tolerances. Since the phase shift correction is based on a time delay, it introduces error when the mains frequency is changed, and this should be taken into account should the mains frequency of the meter change significantly.

A 9-bit signed magnitude value is used to null the phase shift error in steps of one clock cycle. A positive value (bit P8 = 0) adds delay to the current signal, a negative value (bit P8 = 1) adds delay to the voltage signal. A maximum delay of 255 clock cycles either way can be achieved. At 50 Hz this is equivalent to a potential phase angle correction of about 2.5° either way, in steps of roughly 0.01°. Upon device reset the phase angle correction register defaults to zero, so no phase correction is applied by default.

ENERGY MEASUREMENT

Theory

The SA5301A is capable of measuring active and reactive energy. For given instantaneous voltage and current signals v(t) and i(t) the instantaneous active power is calculated as follows:

$$v(t) = V_M \cos(\omega t + \theta)$$

$$i(t) = I_M \cos(\omega t + \psi)$$

$$p(t) = v(t) \times i(t)$$

$$p(t) = V_M \cos(\omega t + \theta) \times I_M \cos(\omega t + \psi)$$

where
V_M is the amplitude of the voltage signal,
I_M is the amplitude of the current signal,
θ is the phase angle of the voltage signal and
ψ is the phase angle of the current signal.

Let $\phi = \theta - \psi$, $V_{RMS} = \frac{V_M}{\sqrt{2}}$ and $I_{RMS} = \frac{I_M}{\sqrt{2}}$ then

$$p(t) = 2 \times V_{RMS} I_{RMS} \times \cos(\omega t + \theta) \times \cos(\omega t + \theta - \phi)$$

which is simplified using a trigonometric product identity

$$p(t) = V_{RMS} I_{RMS} (\cos\phi + \cos(2(\omega t + \theta) - \phi))$$

Integrating the instantaneous active power over time provides the average active power information by removing the double frequency component:

$$P = \frac{1}{T} \int_0^T p(t) dt$$

$$P = V_{RMS} I_{RMS} \cos\phi$$

where
$\cos\phi$ is the power factor.

Likewise the instantaneous reactive power may be calculated by adding a 90° phase shift to the voltage signal before multiplication:

$$q(t) = V_{\mathrm{M}} \cos\left(\omega t + \theta - \frac{\pi}{2}\right) \times I_{\mathrm{M}} \cos\left(\omega t + \psi\right)$$

$$q(t) = 2 \times V_{\mathrm{RMS}} I_{\mathrm{RMS}} \times \sin\left(\omega t + \theta\right) \times \cos\left(\omega t + \theta - \phi\right)$$

$$q(t) = V_{\mathrm{RMS}} I_{\mathrm{RMS}} \left(\sin\phi + \sin\left(2\left(\omega t + \theta\right) - \phi\right)\right)$$

Integrating the instantaneous reactive power over time provides the average power information by removing the double frequency component:

$$Q = \frac{1}{T}\int_0^T q(t)dt$$

$$Q = V_{\mathrm{RMS}} I_{\mathrm{RMS}} \sin\phi$$

Implementation Details

The SA5301A preconditions the voltage signal prior to multiplication. This is done by a cascade of low pass filters and a decimator to remove the high frequency noise from the modulator. Subsequently, the offset of the voltage signals is removed. This offset is a combination of the real offset in the voltage signal and the offset of the modulator. Removing this offset is crucial for energy measurement calculations. The resulting average energy is a DC component signal, that will be influenced by the offset components of the input signals, unless one of them is removed prior to multiplication. The presence of offset cancellation implies that the SA5301A is able to measure AC signals only.

After offset cancellation the voltage signal is up-sampled back to the original sampling rate and multiplied with the current signal. The result is accumulated in the active energy register.

For the reactive energy calculation a 90° phase shift is inserted in the voltage path after offset cancellation. Once again the resulting signal is up-sampled back to the original sampling rate and multiplied with the current signal. This result is accumulated in the reactive energy register.

The SA5301A implements the 90° phase shift by means of a low pass filter operated in deep cut-off. This technique has been proven to be far superior to the time delay method of implementing the 90° phase shift, especially in the presence of harmonics. The phase shifting filter utilizes a unique sampling scheme to ensure that the phase shift and gain remain constant even if the mains frequency changes.

The SA5301A is able to measure active and reactive energy to an accuracy of less than 0.1 % error over a dynamic range of 1000:1.

The offset cancellation and phase shift circuits have been designed to operate in the frequency range of 30 Hz to 100 Hz. Mains frequencies outside this range will cause a reduction in active energy measurement accuracy and the reactive energy calculation algorithm will cease to operate correctly.

Active and Reactive Energy Registers

The active and reactive energy registers (banks 1-3, addresses 0x01 and 0x02 respectively) are 24-bit registers that store the instantaneous energy. They increment over time for positive energy (inductive on reactive) and decrement for negative energy (capacitive on reactive). One register count, i.e. one pulse, is equivalent to a certain amount of measured energy. The register pulse rate is 190 000 pulses per second at maximum rated conditions (200 mV_{RMS} input signal on the voltage and current inputs). In 16-bit read mode the lower 8 bits are ignored, so the pulse rate is 742 pulses per second at maximum rated conditions. The gain of the active and reactive energy calculation algorithms is identical by design, so register pulse rates of the active and reactive registers are identical.

The energy accumulated in a specific time period is determined by the change in the register value over that time. The optional clear-on-read feature is very useful here, simply reading the registers with the clear-on-read enabled returns the energy accumulated since the last register read.

The pulse rate of active and reactive registers is dependent on the bandgap reference voltage, the oscillator frequency as well as the input energy, and can be derived as follows:

$$f_{\mathrm{REG-ACT}} = 4 \times \frac{V_{\mathrm{IN}} \times I_{\mathrm{IN}} \times \cos\phi}{{V_{\mathrm{BG}}}^2} \times f_{\mathrm{OSC}} \qquad (1)$$

$$f_{\mathrm{REG-RCT}} = 4 \times \frac{V_{\mathrm{IN}} \times I_{\mathrm{IN}} \times \sin\phi}{{V_{\mathrm{BG}}}^2} \times f_{\mathrm{OSC}} \qquad (2)$$

where
V_{IN} is the RMS magnitude of the input signal to the voltage modulator,
I_{IN} is the RMS magnitude of the input signal to the current modulator,
ϕ is the phase angle between the voltage and current input signals,
V_{BG} is the value of the bandgap reference voltage (1.225 V nominal) and
f_{OSC} is the oscillator frequency (1.786 MHz nominal).

For a given nominal voltage (V_{NOM}) and maximum current (I_{MAX}), with their associated V_{IN} and I_{IN} amplitudes, the relationship between register counts and energy can be determined as follows (shown for active energy, reactive is similar):

$$\mathrm{pulses/Ws} = \frac{f_{\mathrm{REG-ACT}}}{V_{\mathrm{NOM}} \times I_{\mathrm{MAX}}}$$

$$\mathrm{pulses/Wh} = \frac{f_{\mathrm{REG-ACT}} \times 3600}{V_{\mathrm{NOM}} \times I_{\mathrm{MAX}}}$$

$$\mathrm{pulses/kWh} = \frac{f_{\mathrm{REG-ACT}} \times 3600 \times 1000}{V_{\mathrm{NOM}} \times I_{\mathrm{MAX}}}$$

Performance Tuning

Under certain conditions it may be desirable to fine tune the performance of the active and reactive energy measurement algorithms. The SA5301A allows this by using the channel performance tuning registers (banks 1-3, address 0x39), which allow the following aspects of the energy measurement algorithm to be tuned:

- the balance between the active and reactive gain
- active linearity
- reactive linearity

Any tuning applied affects the energy registers on the SPI interface as well as the pulse output module. At device reset all the channel performance tuning register bits default to zero, so no tuning is applied by default.

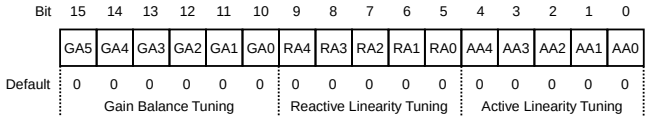


Figure 8: *Channel performance tuning register*

Gain Balance

The gain of the reactive algorithm has been designed to exactly match the active algorithm gain, resulting in equal pulse rates for the active and reactive registers. This means that independent calibration of the active and reactive channels should not be necessary. Both quantities are derived from the same signals, and so should be subject to the same calibration adjustments.

There may however be circuit configurations where this is no longer the case. To ensure that the active and reactive gains can always be matched, bits GA5-GA0 are available. These bits represent a a signed magnitude number between −31 and 31 that allows the gain of the reactive algorithm to be changed. One count represents about 0.03 %, so the total tuning range is approximately ±0.93 %. If GA5 is set, the reactive gain is lowered, it is raised if GA5 is cleared.

Linearity Compensation

Although the active and reactive energy algorithms have been designed for a linearity error of less than 0.1 % over a current range of 1000:1, some residual fixed offsets will always remain. Under certain circumstances it may be desirable to improve the linearity by removing these offsets. The voltage and/or current sensing networks may also give rise to a fixed offset that impacts linearity error. The linearity compensation bits (AA4-AA0 for active and RA4-RA0 for reactive) may be used to remove fixed offsets, thereby improving the observed load linearity.

Linearity compensation is achieved by adding or subtracting a fixed pulse rate from the energy accumulation registers. The compensation bits are signed magnitude numbers between −15 and 15. Each count represents approximately one pulse per 14.4 seconds, or 0.069 pulses per second. Given the nominal pulse rate per register of 190 000 pulses per second at maximum rated conditions or 190 pulses per second at 0.1 % (1/1000th) of rated conditions, 0.069 pulses per second represents approximately 0.036 % at 0.1 % of full-scale range. One correction count therefore implies a fixed error cancellation of 0.036 % at 1/1000th of full-scale.

Fixed offsets of about ±0.55 % can be cancelled. If the sign bit AA4 or RA4 is cleared, energy is added to the register, so a negative offset error can be cancelled. Positive offset errors can be cancelled by setting the sign bit and therefore subtracting energy from the accumulation register.

VOLTAGE AND CURRENT RMS

The SA5301A is able to measure and calculate the RMS values of the voltage and current signals. True RMS calculations are performed, which means that the algorithms are able to handle the presence of harmonics. The results are updated once per mains cycle and stored in the voltage and current RMS registers (banks 1-3, addresses 0x03 and 0x04 respectively). These are 24-bit registers and they store an unsigned positive value that is proportional to the RMS value measured. The actual RMS values for voltage and current can be calculated as follows:

$$S_{\mathrm{RMS}} = \frac{R_{\mathrm{RMS}} \times V_{\mathrm{BG}}}{2^{25.5}} \tag{3}$$

$$\text{Voltage RMS} = \frac{S_{\mathrm{RMS}}}{V_{\mathrm{IN}}} \times V_{\mathrm{NOM}}$$

$$\text{Current RMS} = \frac{S_{\mathrm{RMS}}}{I_{\mathrm{IN}}} \times I_{\mathrm{MAX}}$$

where

S_{RMS} is the RMS magnitude of the input signal to the modulator,

R_{RMS} is the value read from the relevant RMS register,

V_{BG} is the value of the bandgap reference voltage (1.225 V nominal),

V_{IN} is the RMS input signal level to the voltage modulator at the nominal mains voltage V_{NOM} of the meter and

I_{IN} is the RMS input signal level to the current modulator at the maximum mains current I_{MAX} of the meter.

At maximum rated input conditions to the modulator of 200 mV_{RMS} input signal the register value will be 7 747 450.

Some low pass filtering is included in the RMS algorithms to ensure more stable and less noisy readings. These filters have a settling time before any changes on the voltage and current inputs are correctly reflected in the register values. The register values settle to 95 % of their final value within 10 mains cycles, and 99 % of their final value within 16 mains cycles.

The output of the offset cancellation circuit on the voltage path is used as input to the voltage RMS calculation. On the current path a similar cascade of filters with a decimator and offset cancellation is used. The need for removing the modulator offset is critical to algorithm accuracy, because any offset, whether introduced via the external signal or from the inherent offset of the modulators, will affect the results of the RMS calculation. The current RMS value is accurate to an error of less than 0.5 % over a dynamic range of 1000:1. The voltage signal has a low dynamic range requirement, as such the voltage RMS value is accurate to an error of less than 0.5 % over a dynamic range of 50:1.

In order to operate correctly, the RMS algorithms require either a stable voltage or current input signal. They are mains cycle based and need to be able to extract the mains cycle timing from one of the incoming signals. As mentioned previously, each measurement channel operates independently, so the mains timing is not shared. If the RMS values cannot be accurately determined due to missing voltage and current signals, the register values default to zero. Refer to the Mains synchronization status flags for additional detail.

Current RMS Offset Mode

The voltage RMS calculation will reject DC in order to achieve good accuracy, a direct consequence of using the output of the offset cancellation circuit on the voltage path as an input. The DC rejection is not considered a problem, the mains voltage signal typically has very little harmonic influences. This is less true for the current signal, high harmonic content and relevant DC offsets may be present, i.e. the extreme case of a half wave rectified current signal. By default the DC offsets in the signal are rejected, just like on the voltage path, which will lead to an incorrect current RMS reading if the signal DC offset is substantial.

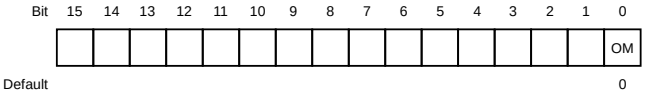


Figure 9: *Channel settings register*

The current RMS calculation can therefore be configured to selectively include or reject the DC component of the input signal, by using the OM bit of the channel settings registers (banks 1-3, address 0x3a). To include the signal DC offset the OM bit should be set, clearing the OM bit will reject the signal DC component. Regardless of the OM bit setting, the DC offset of the modulator will always be rejected to maintain the accuracy of the RMS calculation algorithm.

Enabling the OM bit has some minor drawbacks. The accuracy of the current RMS measurement is slightly affected and the active and reactive measurements tend to be more noisy at very low currents. Disabling the OM bit rejects all DC offsets, and produces the best accuracy results, even at very low mains currents. The OM bit can be changed on the fly if required, the SA5301A circuitry will ensure that the changes are correctly synchronised to the algorithm, allowing a combination of the two schemes to be used for best overall performance.

MAINS PERIOD AND PHASE ANGLE

The SA5301A can use the zero crossings of the mains voltage and current signals to extract the mains period as well as the phase angle between the voltage and current signals. The mains period is measured by counting the number of device clock cycles per mains cycle. This result is stored in the 16-bit mains period registers (banks 1-3, address 0x05) as an unsigned positive value. The mains period is extracted from the voltage input signal by default. Should this signal be too small the current input signal can be used if it is large enough. If both signals are too small (typically less than 1 % full-scale), the mains period cannot be extracted and the mains period register will default to zero. Refer to the Mains synchronization status flags for additional detail.

$$\text{Mains Period} = \frac{R_{\text{Period}}}{f_{\text{OSC}}}$$

where
R_{Period} is the value read from the relevant mains period register and
f_{OSC} is the oscillator frequency (1.786 MHz nominal).

The phase angle is presented as a 16-bit 2's complement integer in the phase angle registers (banks 1-3, address 0x06) and represents the number of clock cycles between the rising zero crossings of the mains voltage and mains current signals. A positive value means that the voltage crossing has occurred before the current crossing, so power factor is lagging. A negative value implies a leading power factor, the current crossing has occurred before the voltage crossing. A value of −32 768 (0x8000) means that the phase angle could not be determined. This will occur if either the mains voltage or current signals are too small to allow reliable zero crossing detection, typically at about 1 % of full-scale on the voltage channel and 0.05 % of full-scale on the current channel. The phase angle in degrees may be calculated as follows:

$$\text{Phase Angle} = \frac{R_{\text{Phase}}}{R_{\text{Period}}} \times 360^{\circ}$$

where
R_{Phase} is the value read from the relevant phase angle register and
R_{Period} is the value read from the relevant mains period register.

A phase angle measurement always includes a discontinuity at some point. This discontinuity has been placed at the

190°/−170° boundary with a fair amount of hysteresis to either side. This implies that phase angles in the range from −180° to −160° may also be indicated as a phase angle in the range of 180° to 200°. At very small current RMS values the phase angle measurement suffers from fairly noisy measurements and reduced accuracy.

VOLTAGE AND CURRENT MONITORING

The SA5301A is able to monitor various aspects of the mains voltage and mains current conditions. Parameters including

- voltage and current zero crossing,
- voltage and current instantaneous polarity,
- missing phase voltage,
- phase sequence error,
- over-voltage,
- under-voltage,
- over-current,
- no-load and
- energy quadrant

are continuously monitored and updated in the bank status registers. A change in any of these conditions may be configured to generate an interrupt. Some of these conditions are fixed in the way they operate, while others are adjustable. The voltage status parameters and current status parameters registers (banks 1-3, addresses 0x3c and 0x3d respectively) allow the adjustment of the monitoring parameters.

Voltage Status Parameters Registers

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OV5	OV4	OV3	OV2	OV1	OV0	UV5	UV4	UV3	UV2	UV1	UV0	ZV3	ZV2	ZV1	ZV0
Default	1	1	1	1	0	0	1	0	0	0	0	0	1	0	0	0
	Over-Voltage Threshold						Under-Voltage Threshold						Missing Phase Threshold			

Figure 10: *Voltage status parameters register*

Each measurement channel of the SA5301A analyses the output of the offset cancellation circuit on the voltage path on a continuous per mains cycle basis. The signal is rectified and the magnitude represented as a 6-bit value. The peak magnitude is determined over one mains cycle and compared to various thresholds to determine the missing phase, under-voltage and over-voltage conditions. Each threshold has 0.5 LSB of hysteresis added, to prevent unstable behaviour of the status bits when the signal peak is very close to the threshold. A specific status condition is only updated if the threshold comparison has been identical for 4 consecutive mains cycles. Independent thresholds can be set for each measurement channel. Note that the comparisons operate on signal peak value, not signal RMS value. The thresholds represent a fraction of the full-scale input signal of 300 mV.

- ***ZV3-ZV0*** - *Missing phase detection threshold:* 4 bits used to set the required 6-bit missing phase detection threshold. ZV5 and ZV4 of the threshold cannot be specified, they are assumed to be zero. The missing phase indication in the relevant bank status register will be set if the peak voltage value does not exceed the threshold. The default value for these bits is 8, setting the default missing phase threshold at 12.5 % (8/64) of the full-scale input signal level.
- ***UV5-UV0*** - *Under-voltage threshold:* 6 bits used to set the required under-voltage detection threshold. The under-voltage indication in the relevant bank status register will be set if the peak voltage value does not exceed the threshold. The default value for these bits is 32, setting the default under-voltage threshold at 50 % (32/64) of the full-scale input signal level.
- ***OV5-OV0*** - *Over-voltage threshold:* 6 bits used to set the required over-voltage detection threshold. The over-voltage indication in the relevant bank status register will be set if the peak voltage value exceeds the threshold. The default value for these bits is 60, setting the default over-voltage threshold at 94 % (60/64) of the full-scale input signal level.

Current Status Parameters Registers

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OC5	OC4	OC3	OC2	OC1	OC0		NLM	NL7	NL6	NL5	NL4	NL3	NL2	NL1	NL0
Default	1	1	1	1	0	0		0	0	1	1	0	0	0	0	0
	Over-Current Threshold							No-Load Threshold								

Figure 11: *Current status parameters register*

- ***NLM and NL7-NL0*** - *No-load threshold:* 9 bits to set the required 20-bit no-load threshold as follows:
  NLM = 0: Threshold is 0000 0000 0000 XXXX XXXX
  NLM = 1: Threshold is 0000 0000 XXXX XXXX 0000
  X represents the NL7 to NL0 bits and NLM is the range multiplier bit which increases the threshold by a factor 16 if set.
  The RMS value of the current signal is used for determining the no-load condition. The upper 20 bits of the current RMS register are checked and compared to the threshold. If this value is less than the threshold, the no-load condition is indicated in the relevant bank status register. A 12.5 % hysteresis is added to the threshold to ensure that the no-load condition is stable. Additionally the no-load status flag is only changed if the detection outcome has been stable for 8 consecutive mains cycles. At maximum rated conditions of 200 mV_{RMS} input signal the current RMS register value will be 7 747 450, as per Equation (3), which is 46.2 % of the full-scale current RMS register value of 2^{24}-1. The default value for the NLM and NL7-NL0 bits is 96 with no multiplier, setting the default no-load threshold at 16×96/7 747 450, roughly 0.02 % of maximum rated RMS current. The factor 16 is required to compensate for the lower 4 bits of the RMS register that are not used in

the comparison. The range of possible threshold values covers a no-load threshold range of 0.84 % of rated input almost down to zero. The no-load threshold will not be very accurate at extremely low threshold values.

- ***OC5-OC0*** *- Over-current threshold:* 6 bits used to set the required over-current detection threshold. An identical peak detection as described in the previous section on the voltage status parameters is used. The output of the offset cancellation circuit on the current path (the same signal used for the current RMS calculation) is rectified and converted to a 6-bit value, which is compared to the over-current threshold. The over-current indication in the relevant bank status register will be set if the peak current signal value exceeds the threshold for 4 consecutive mains cycles. Again note that the over-current detection operates on peak signal value, not RMS signal value. The default value for the OC5-OC0 bits is 60, setting the default over-current threshold at 94 % (60/64) of the full-scale input signal level.

TIME REFERENCE REGISTER

The time reference register (bank 0, address 0x1f) simply counts device clock cycles and can be read with or without clear. When using the clear-on-read feature this register allows simple determination of the elapsed device clock cycles since the last read. The time reference register can count up to 2^{24} clock cycles and will therefore overflow after approximately 9.4 s. This register can be useful in accurately determining elapsed time with the on-chip oscillator as a base reference. Alternatively it can provide the number of device clock cycles within a predetermined time when performing additional calibration to null the effect of variations in the on-chip oscillator. When reading this register in 16-bit mode the least significant bit represents 256 clock cycles.

PULSE OUTPUT MODULE

Generating active and reactive output pulses is often a required feature for any energy metering system. This can typically be done using the micro-controller but generating accurate pulses can be a time critical task that consumes a large portion of micro-controller resources. The SA5301A includes a highly configurable pulse output module for generating active and reactive pulse outputs, in order to relieve the system micro-controller of this task. Alternatively, the pulse output module can allow the SA5301A to operate in a stand-alone mode, measuring energy and generating the required pulse outputs.

Overview

The pulse output module on the SA5301A produces active and reactive pulse outputs. The block diagram in Figure 12 shows the signal path for the active output pulses. The reactive path is identical. The incoming measured energy from one measurement channel is multiplied with a calibration constant set by the calibration register in the relevant channel. The same calibration constant is used for both the active and reactive pulse generation. Separate calibration constants are not required as the incoming pulse rates for active and reactive are identical. A low pass filter on a per-channel basis ensures smooth output pulses. The three channels are added together by means of a programmable adder.

The pulse generation block uses a configurable divider to adapt the pulse output rate. This divider is unique to the active and reactive paths, allowing different base pulse rates on active and reactive output pulses. The default divider is set to produce output pulses of 5 kHz at nominal input conditions. A post divider allows further reduction in the pulse output rate in steps of 2^n from 1 to 2^{15}. Frequencies as low as 0.05 Hz at nominal input conditions can be achieved using the combination of available dividers. The final block is the output formatter that generates the actual output pulses to the required format. Various options exist for formatting the output pulses, as described later.

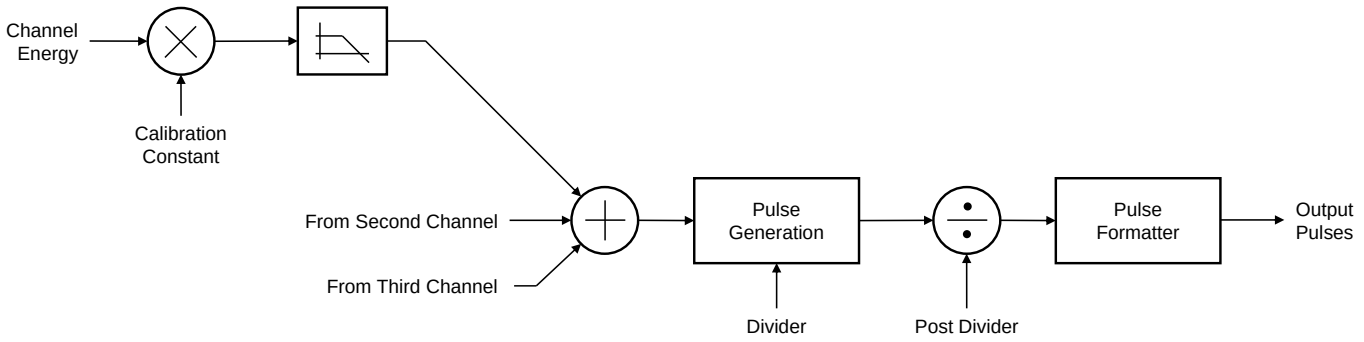


Figure 12: *Pulse output module block diagram*

Pulse Output Calibration Registers

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0
Default			1	1	0	0	0	0	0	0	0	0	0	0	0	0

Figure 13: *Pulse output calibration register*

The pulse outputs calibration registers (banks 1-3, address 0x20) hold a 14-bit value to ensure adequate calibration accuracy. Their default value is 0x3000, 12 288. The range of applicable values that can be written to the registers is between 0x0200 and 0x3dff, values outside this range will not be written to the registers. This allows for a calibration constant in the range 512 to 15 871, creating a calibration range of a factor 31. For best accuracy at low energy levels the downstream dividers (pulse generation divider and post divider) should be chosen to obtain the largest possible calibration constant. Each measurement channel of the SA5301A has a unique separate calibration constant, however the same constant is used for both active and reactive pulses on a channel.

Pulse Output Divider Registers

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DP3	DP2	DP1	DP0	AM1	AM0	DG9	DG8	DG7	DG6	DG5	DG4	DG3	DG2	DG1	DG0
Default	0	0	0	0	0	0	1	0	1	0	1	0	1	1	0	1
	Post Divider				Adder Mode		Divider									

Figure 14: *Pulse output divider register*

The pulse generation divider and post divider as well as the programmable adder mode are set by means of the pulse output divider registers (bank 0, addresses 0x21 and 0x22). One register is used for the active channel (address 0x21), the other for the reactive channel (address 0x22).

- ***DG9-DG0*** *- Pulse generation divider:* These 10 bits set the divider for the pulse generation. This divider can be set in a range of 0x100 (256) to 0x37f (895) and the default value is 0x2ad (685). The true divider used is this value multiplied by 2^{11}. The default value produces 5 kHz output pulses with a post divider of 1 at nominal input conditions.
- ***AM1, AM0*** *- Adder mode:* These 2 bits set the mode of the programmable adder that adds the three measurement channels together.
  - 00 - Arithmetic mode, the three channels are added together taking the direction of energy flow into account. Negative energy on one channel is thus subtracted from positive energy on a different channel
  - 01 - Absolute mode, the three channels are added together disregarding the direction of energy flow. The absolute value of the energy on each channel is determined prior to addition. This mode will always produce positive output pulses.
  - 10 - Positive only, only positive energy (inductive in the case of the reactive pulse output) is added, negative energy is ignored. This mode only produces positive output pulses.
  - 11 - Negative only, only negative energy (capacitive in the case of the reactive pulse output) is added, positive energy is ignored. This mode only produces negative output pulses.
- ***DP3-DP0*** *- Post divider:* These 4 bits are interpreted as a value n from 0 to 15 which sets the post divider to 2^n.

The active pulse output frequency is determined by the following equation:

$$f_{\mathrm{OUT-ACT}} = \frac{f_{\mathrm{ACT1}} \times CC_1 + f_{\mathrm{ACT2}} \times CC_2 + f_{\mathrm{ACT3}} \times CC_3}{2^{11} \times DG_{\mathrm{ACT}} \times 2^{DP_{\mathrm{ACT}}}}$$

where
f_{ACT1}, f_{ACT2} and f_{ACT3} are the active register pulse rates as per Equation (1)
CC_1, CC_2 and CC_3 are the pulse output calibration register values of the respective measurement channels
DG_{ACT} is the active pulse generation divider value and
DP_{ACT} is the active post divider n-value.

Similarly, the reactive pulse output frequency is determined by:

$$f_{\mathrm{OUT-RCT}} = \frac{f_{\mathrm{RCT1}} \times CC_1 + f_{\mathrm{RCT2}} \times CC_2 + f_{\mathrm{RCT3}} \times CC_3}{2^{11} \times DG_{\mathrm{RCT}} \times 2^{DP_{\mathrm{RCT}}}}$$

where
f_{RCT1}, f_{RCT2} and f_{RCT3} are the reactive register pulse rates as per Equation (2)
CC_1, CC_2 and CC_3 are the pulse output calibration register values of the respective measurement channels
DG_{RCT} is the reactive pulse generation divider value and
DP_{RCT} is the reactive post divider n-value.
The above equations are valid with the adder mode set to arithmetic sum. They need to be modified accordingly as per the adder mode description if the adder mode is changed.

The combination of the post divider and the pulse generation divider together with the calibration constants allows any desired output pulse rate down to about 0.1 Hz at nominal input conditions to be set. Pulse rates above 7.5 kHz should be avoided.

Pulse Output Setup Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								NL	MP	C3	C2	C1	RVP	W1	W0	LEV
Default								0	0	1	1	1	0	0	0	0

Figure 15: *Pulse output setup register*

Various options that control the format of the output pulses and some global settings for the pulse output module can be set using the pulse output setup register (bank 0, address 0x23).

- ***LEV*** *- Pulse level:* This bit sets pulses to active low when set and active high when cleared.
- ***W1, W0*** *- Pulse width:* These bits set the pulse width as follows
  - 00 - 71.7 µs
  - 01 - 4.59 ms
  - 10 - 147 ms
  - 11 - 50 % duty cycle

  The pulse width defaults to 50 % duty cycle if the pulse output rate is too high to accommodate the selected pulse width. The pulse width will never exceed 50 % of the pulse period.
- ***RVP*** *- Reverse pulse width:* When this bit is set the pulse width for reverse energy pulses (capacitive pulses on reactive) is 1.5 times the selected pulse width. This does not apply if a 50 % duty cycle pulse width is selected or the pulse output rate is too high to accommodate the required output pulse width.
- ***C3, C2, C1*** *- Channel selection bits:* These three bits enable each of the 3 measurement channels to contribute energy to the pulse outputs. Energy from a disabled channel does not contribute to pulse generation, however all other aspects of the channel remain fully functional.
- ***MP*** *- Enable missing phase:* If this bit is set the energy from a specific measurement channel will not be added to the pulse output if the missing phase condition has been detected on that channel.
- ***NL*** *- Enable no-load:* If this bit is set the energy from a specific measurement channel will not be added to the pulse output if the no-load condition has been detected on that channel.

DEVICE STATUS AND INTERRUPTS

The SA5301A is able to continuously monitor various aspects of the device operation, mains voltage and mains current conditions. The results are updated in the bank status registers and the global status register. A change in any of the monitored conditions may be configured to generate an interrupt to the micro-controller. Some of these conditions are fixed in the way they operate, others are adjustable.

The SA5301A contains 4 status registers, one in each bank. The three located in banks 1 to 3 provide status information from their respective measurement channel. The fourth is a common status register, it holds information that has been combined from the bank status registers as well as some additional information. All 4 status registers are 16 bit readable.

Bank Status Registers

Each independent measuring channel of the SA5301A contains a status register, the bank status register (banks 1-3, address 0x00). It holds status flags that are relevant to that channel only.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				SF2	SF1	Q1	Q0	OV	UV	MP	OC	NL	VZ	CZ	VP	CP

Figure 16: *Bank status register*

- ***CP*** *- Current signal polarity:* This bit indicates the instantaneous polarity of the current signal, it is set if the current signal is positive, it is cleared if the current signal is negative.
- ***VP*** *- Voltage signal polarity:* This bit indicates the instantaneous polarity of the voltage signal, it is set if the voltage signal is positive, it is cleared if the voltage signal is negative.
- ***CZ*** *- Current zero crossing:* A 1.15 ms pulse is generated in this bit at each rising zero crossing detected on the current signal.
- ***VZ*** *- Voltage zero crossing:* A 1.15 ms pulse is generated in this bit at each rising zero crossing detected on the voltage signal.
- ***NL*** *- No-load:* This flag is set if the no-load condition is detected.
- ***OC*** *- Over-current:* This flag is set if the over-current condition is detected.
- ***MP*** *- Missing phase:* This flag is set if the missing phase condition is detected.
- ***UV*** *- Under-voltage:* This flag is set if the under-voltage condition is detected.
- ***OV*** *- Over-voltage:* This flag is set if the over-voltage condition is detected.
- ***Q1, Q0*** *- Energy quadrant:* These 2 flags indicate in which of the four quadrants the energy flow is being measured. Q0 is set if export energy is detected, Q1 is set if capacitive reactive energy is measured. Therefore the quadrants are indicated as follows:
  - quadrant 1 - 00 (import, inductive)
  - quadrant 2 - 01 (export, inductive)
  - quadrant 3 - 11 (export, capacitive)
  - quadrant 4 - 10 (import, capacitive)
- ***SF2, SF1*** *- Mains synchronization:* Many aspects of the SA5301A circuitry rely on a steady mains voltage signal being present in order to operate correctly. The most relevant circuits are the offset cancellation, the reactive energy algorithm and the RMS calculation algorithm. If a stable mains voltage signal of significant amplitude is not present then these circuits would cease to operate correctly. This is typically a robust scenario, the lack of a mains voltage means that no current can flow, so no energy flow can be recorded on that measurement channel. It could however also represent a tamper condition. To counter this, the mains synchronization can also be extracted from the current signal, provided it has sufficient amplitude. This allows the algorithms to continue functioning, albeit at slightly degraded performance. Whenever the measurement channel is synchronizing from

the current signal, the sync flag SF2 will be set. Most importantly, current RMS will continue to function correctly, so energy usage could be inferred and billed from the current RMS magnitude. If a valid synchronization cannot be extracted from either the voltage or current signal then various algorithms will cease to function (RMS and reactive energy) or will operate at degraded performance (offset cancellation). This is indicated by SF1 being set.

The flags NL, OC, MP, UV and UC can be instantaneous or latching. In instantaneous mode the flags indicate the present state of their status condition detectors. In latching mode a flag will be set when a status condition is detected and will remain set even if the status condition is no longer detected. The bank status register needs to be read to clear a latched status flag. The flag will only be cleared on read if the relevant status condition is no longer present. The latching status flag feature is configured in the status and interrupt setup register.

Global Status Register

The global status register (bank 0, address 0x00) combines status flags from the three bank status registers together and also features some additional status bits. Each measurement channel can be individually enabled or disabled when merging the bank status register bits, refer to the status and interrupt setup register for more information.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INT	RST	RCT	ACT	SF	PSE	REV	OV	UV	MP	OC	NL	VZ	CZ	VP	CP

Figure 17: *Global status register*

- ***CP*** *- Current signals polarity:* This bit indicates the combined instantaneous polarity of the current signals. It is the logical XOR of the CP bits of all enabled bank status registers.
- ***VP*** *- Voltage signals polarity:* This bit indicates the combined instantaneous polarity of the voltage signals. It is the logical XOR of the VP bits of all enabled bank status registers.
- ***CZ*** *- Current zero crossings:* This bit is the logical OR of the CZ bits of all enabled bank status registers.
- ***VZ*** *- Voltage zero crossings:* This bit is the logical OR of the VZ bits of all enabled bank status registers.
- ***NL*** *- No-load:* This flag is the logical OR of the NL flags of all enabled bank status registers.
- ***OC*** *- Over-current:* This flag is the logical OR of the OC flags of all enabled bank status registers.
- ***MP*** *- Missing phase:* This flag is the logical OR of the MP flags of all enabled bank status registers.
- ***UV*** *- Under-voltage:* This flag is the logical OR of the UV flags of all enabled bank status registers.
- ***OV*** *- Over-voltage:* This flag is the logical OR of the OV flags of all enabled bank status registers.
- ***REV*** *- Reverse energy:* This flag is the logical OR of the Q0 flags of all enabled bank status registers. While the Q0 flags of the bank status registers are instantaneous, the REV flag can be set to latching mode, so an export energy condition on any of the enabled bank status registers is latched until the global status register is read.
- ***PSE*** *- Phase sequence error:* This flag is set if the rising zero crossings on the voltage signals follow the 132 sequence instead of the correct 123 sequence, indicating a reversed phase sequence. The PSE flag can be instantaneous or latching. In the latter case it can be cleared by reading the global status register. This flag is only valid if all three mains voltage signals are valid. If this is not the case, the PSE flag will default to clear.
- ***SF*** *- Synchronization:* This flag is the logical OR of the SF1 and SF2 flags of all enabled bank status registers.
- ***ACT*** *- Active pulse:* This bit is the active pulse output from the pulse output module. The bit is set during the active period of the active pulse output
- ***RCT*** *- Reactive pulse:* This bit is the reactive pulse output from the pulse output module. The bit is set during the active period of the reactive pulse output
- ***RST*** *- Reset:* This flag is set when the device is in reset, it is always latching and can be cleared by reading the global status register. If the RST flag is ever set again after being initially cleared, it indicates there must have been a power glitch that has reset the SA5301A. The settings will also have been reset to their default value if this is the case, and would need to be refreshed.
- ***INT*** *- Interrupt:* This flag is set if an interrupt is detected. The interrupt detection circuitry is configurable, refer to the status and interrupt setup register for more information.

Status Bits Summary

The table below has a summary of the functionality of all the status flags. Those flags in the global status register that are a combined version of bank status flags are not included, their characteristics are derived from the respective source flags.

Table 2: *SA5301A status bits summary*

Flag	Location	Detection Time	Type	Notes and Special Cases
CP	Bank	~150 µs after signal crossing	Instantaneous	1. Valid voltage synchronization (SF1 and SF2 clear): Retains last state when the mains current signal becomes too small, typically about 1/2500th of full-scale. 2. No synchronization (SF1 set): Retains last state
VP	Bank	~150 µs after signal crossing	Instantaneous	Retains last state when the mains voltage signal is invalid (SF2 or SF1 set)
CZ	Bank	~150 µs after signal crossing	1.15 ms pulse	Derived from CP, so no pulses emitted if CP does not toggle
VZ	Bank	~150 µs after signal crossing	1.15 ms pulse	Derived from VP, so no pulses emitted if CP does not toggle
NL	Bank	8 mains cycles	Instantaneous or latching	Cleared when no synchronization is detected (SF1 set)
OC	Bank	4 mains cycles	Instantaneous or latching	Cleared when no synchronization is detected (SF1 set)
MP	Bank	4 mains cycles	Instantaneous or latching	Always valid
UV, OV	Bank	4 mains cycles	Instantaneous or latching	Cleared when invalid mains voltage signal is detected (SF2 or SF1 set)
Q0, Q1	Bank	8 mains cycles	Instantaneous	Cleared when invalid mains voltage signal is detected (SF2 or SF1 set) or no-load condition is present (NL set)
SF1	Bank	1 mains cycle	Instantaneous	Always valid
SF2	Bank	4 current mains cycles	Instantaneous	Always valid
REV	Global	8 mains cycles	Instantaneous or latching	Derived from Q0 in each bank status register
PSE	Global	5 mains cycles	Instantaneous or latching	Cleared when invalid mains voltage signal is detected on any phase (any SF1 or SF2 set)

Interrupts

An interrupt can be generated from almost any bit of the global status register, except the interrupt flag itself and the voltage and current polarity bits. The Reset flag, RST, always generates an interrupt, all other flags are configurable. If a certain bank status register is not enabled to propagate its flags to the global status register, that measurement channel cannot generate an interrupt via its status flags. The status and interrupt setup register (bank 0, address 0x3f) is used to configure bank status register merging and the generation of interrupts.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IM	PR	PA	SF	PSE	REV	VS	MP	OC	NL	VZ	CZ	C3	C2	C1	FL
Default	0	0	0	1	1	1	1	1	1	1	0	0	1	1	1	0

Figure 18: *Status and interrupt setup register*

- ***FL*** *- Flags latching:* Setting this bit sets the relevant status flags in the bank status registers and the global status register to latching mode. Clearing this bit sets all status flags to instantaneous mode.
- ***C1*** *- Enable channel 1 status:* Setting this bit allows the bank status register bits of measurement channel 1 to propagate to the global status register.
- ***C2*** *- Enable channel 2 status:* Setting this bit allows the bank status register bits of measurement channel 2 to propagate to the global status register.
- ***C3*** *- Enable channel 3 status:* Setting this bit allows the bank status register bits of measurement channel 3 to propagate to the global status register.
- ***CZ*** *- Current zero crossing enable:* Setting this bit allows the current zero crossing status bit to generate an interrupt.
- ***VZ*** *- Voltage zero crossing enable:* Setting this bit allows the voltage zero crossing status bit to generate an interrupt.
- ***NL*** *- No-load enable:* Setting this bit allows the no-load status flag to generate an interrupt.

- ***OC** - Over-current enable:* Setting this bit allows the over-current status flag to generate an interrupt.
- ***MP** - Missing phase enable:* Setting this bit allows the missing phase status flag to generate an interrupt.
- ***VS** - Voltage status enable:* Setting this bit allows the under-voltage and over-voltage status flags to generate an interrupt.
- ***REV** - Reverse energy enable:* Setting this bit allows the reverse indication status flag to generate an interrupt.
- ***PSE** - Phase sequence error enable:* Setting this bit allows the phase sequence error status flag to generate an interrupt.
- ***SF** - Sync flag enable:* Setting this bit allows the synchronization status flag to generate an interrupt.
- ***PA** - Active pulse enable:* Setting this bit allows the active pulse signal to generate an interrupt. The interrupt is generated for the active period of the output pulse signal.
- ***PR** - Reactive pulse enable:* Setting this bit allows the reactive pulse signal to generate an interrupt. The interrupt is generated for the active period of the output pulse signal.
- ***IM** - Interrupt mode setup:* This bit determines the behaviour of the interrupt flag.
  - 0 - Direct: When IM is cleared the behaviour is direct, and is essentially the logic OR of all the interrupt enabled status bits. Therefore the flag will only be cleared when all enabled interrupt status bits are not active.
  - 1 - Pulse: A 1.15 ms pulse is generated on the interrupt flag when any enabled interrupt condition becomes active. The interrupt signal will always be active for 1.15 ms after the last interrupt has been detected. Multiple interrupts occurring within 1.15 ms of each other will therefore not generate multiple pulses, they will extend the pulse width of the INT signal.

CONFIGURABLE OUTPUT PINS

The SA5301A has four dedicated output pins (CA, CB, CC and CD) that can be configured to output any one of the status bits of the global status register. The configuration is done by means of the configurable outputs setup register (bank 0, address 0x3e). Four bits are allocated to each output pin and must contain the bit address of the global status bit desired on the output pin. For example, the four bits PA3-PA0 are programmed with a number between 0 and 15 to determine which of the global status bits 0 to 15 appears on CA. The default condition of this register is designed to output active pulses on CA, reactive pulses on CB, mains zero crossing on CC and the interrupt signal on CD.

The configurable output pins are capable of directly driving loads of up to 15 mA, if more output current is required an external buffer is recommended.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PD3	PD2	PD1	PD0	PC3	PC2	PC1	PC0	PB3	PB2	PB1	PB0	PA3	PA2	PA1	PA0
Default	1	1	1	1	0	0	1	1	1	1	0	1	1	1	0	0
	CD Setup				CC Setup				CB Setup				CA Setup			

***Figure 19:** Configurable outputs setup register*

SPI INTERFACE

The SA5301A has a 4-wire serial interface that is compatible with the standard SPI interface specification. The SPI interface is used to access the registers on the device. A module using a cyclic redundancy check code (CRC) is present to allow communication errors on the SPI interface to be detected. Different register reading modes can be enabled to optimize the read-out of measurement data to suit the application needs.

SPI Signals

The SPI interface consists of 4 signals:

- ***CS** - Chip select:* Active high enable signal to indicate the start and end of an SPI transaction. The device ignores the clock and data input and leaves the data output floating when CS is low. This allows multiple SPI compatible devices to share the same SCK, MOSI and MISO lines.
- ***SCK** - Serial clock:* The clock signal for data transactions. Data is sampled on the data input and driven on the data output (if required) on the rising edge of SCK when CS is high.
- ***MOSI** - Master out, slave in:* The data input to the SA5301A.
- ***MISO** - Master in, slave out:* The data output of the SA5301A. This pin is floating unless register data is actively being read from the device.

In order to be compatible with other SPI devices, the SPI pins have no internal pull-up or pull-down resistors. If any of the SPI signals can float or are unused, an external pull-up or pull-down resistor must be added to ensure that the signal levels remain within the digital IO specification. The MISO signal floats unless data is being read from the SA5301A, so a pull-up or pull-down resistor is always required. Suggested values for the resistors are in the 100 kΩ range to limit power waste, but they can be smaller if required by other devices connected to the SPI bus.

Table 3: SPI timing constraints

Constraint	Description	Min	Max	Comment
t1	SCK rising edge to MISO valid	530 ns	1.18 µs	minimum 1, maximum 2 device clock cycles
t2	CS and MOSI setup time	50 ns		
t3	SCK minimum high time	590 ns		minimum 1 device clock cycles
t4	SCK minimum low time	590 ns		minimum 1 device clock cycles
t5	CS and MOSI hold time	590 ns		minimum 1 device clock cycles

SPI Timing

The SA5301A samples CS, MOSI and SCK using the device system clock. A rising clock edge on SCK is therefore detected within 1 device clock cycle. Setup times on CS and MOSI are not critical, but should not be zero to account for signal delay differences. The hold times must be at least one device clock cycle, CS and MOSI need to still be valid when SCK is sampled. It takes one additional device clock cycle to process the rising clock edge and update the MISO output. The SCK high and low times need to be at least one device clock cycle each, refer to Figure 20 in conjunction with Table 3 for more detail on the SPI timing.

The device clock cycle time depends on the on-chip oscillator and the external resistor used. The default is 1.786 MHz, but a ±5 % tolerance should be catered for. It is suggested to keep the SPI clock frequency below 800 kHz.

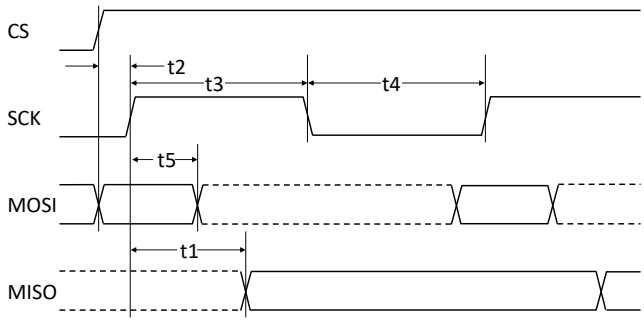


***Figure 20:** SPI timing diagram*

SPI Header

Each SPI data transaction is preceded by a header which is generated and sent by the SPI master. This header instructs the SA5301A on what type of data transaction is to follow. The header contains 4 fields and is 14 bits in length, but may be increased to any larger length by padding it with leading zeros.

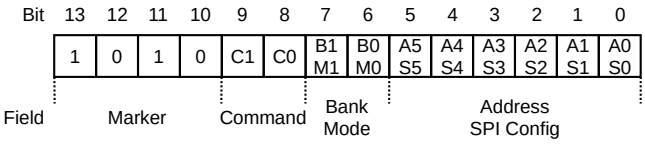


***Figure 21:** SPI header structure*

- ***Marker**:* The device samples the MOSI line on the rising SPI clock edge while CS is high. All data is ignored until the marker sequence is detected. The search for this marker sequence allows the header length to be extended as long as the preceding data does not contain the marker sequence. Once the marker sequence is detected the SA5301A samples 10 additional bits to complete the header.
- ***Command**:* The two command bits determine which type of transaction is being initiated.
  - 00 - SPI Config: the SPI configuration bits can be written and/or the SPI CRC register can be read. In this mode the bank bits and address bits form the SPI mode and config bits respectively.
  - 01 - SPI Write: the device register being addressed will be written to
  - 10 - SPI Read: the device register being addressed will be read
  - 11 - SPI Read with clear: the device register being addressed will be read and its contents cleared. This is not applicable to all registers, only those that operate as accumulators, the energy registers and the time reference register. If a register does not have a clear-on-read function, then this command is interpreted as a normal read command.
- ***Bank**:* These two bits determine the register bank of the device being addressed
  - 00 - Common: contains the registers that are not linked to a specific measurement channel of the device
  - 01 - Phase 1: measurement channel 1
  - 10 - Phase 2: measurement channel 2
  - 11 - Phase 3: measurement channel 3
- ***Address**:* These six address bits allow up to 64 registers to be addressed per bank.

SPI Mode and Settings Bits

The 2 SPI mode and 6 SPI settings bits replace the bank and address bits in the SPI header when using the SPI Config command. They are used to configure how the SPI interface operates. The default state of all settings bits is zero.

SPI Settings Bits

- ***S1, S0** - Register access mode:* These two bits determine how many bits are read out per register when reading registers.

- 00 - all registers are read out using 24 bits per register. The 16-bit registers have 8 leading zeroes added to the register data.
- 01 - all registers are read out using 16 bits only. All 24-bit registers will have their lower 8 bits truncated.
- 1X - all registers are read out based on their native resolution.

- ***S3, S2*** *- Register cycle mode:* these two bits determine how registers are cycled when multiple registers are read in one transaction.
  - 00 - cycle all readable registers
  - 01 - cycle all readable registers within the addressed bank
  - 10 - cycle through all banks, keeping the register address constant, if a certain address in not implemented in a specific bank, that bank is skipped.
  - 11 - cycle only the addressed register
- ***S4*** *- CRC header mode:* This bit determines if the SPI header data is part of the CRC calculation or not. If the bit is set both the header and the register data are used, if cleared only the register data is used for the CRC calculation. The actual CRC register is never included to prevent the CRC register from overflowing.
- ***S5*** *- Unused:* This bit should remain zero at all times

SPI Mode Bits

- ***M0*** *- Enable settings bits write:* This bit must be set to allow the SPI settings bits (S5-S0) to be written. The SPI settings bits will not be written if M0 is not set. Keeping this bit clear allows reading of the CRC register without modifying the SPI setting bits, irrespective of the actual bit values for (S5-S0) in the SPI header.
- ***M1*** *- Initialize CRC register:* If this bit is set, the CRC register will be reset to its initial value after the config transaction completes, when CS goes low.

SPI Transactions

All SPI transactions start with sending the 14 header bits, MSB first, to the SA5301A followed by the relevant data exchange. A transaction may be terminated at any time by pulling CS low.

Read

Figure 22 illustrates a multi register read transaction. After the 14 header bits have been received by the SA5301A, the data of the register being addressed is clocked out on MISO, MSB first. The number of bits being clocked out depends on the SPI setting bits S3 and S2. Once all bits of the addressed register have been clocked out (XN-X0), the next register in the configured sequence is clocked out (YN-Y0). This process continues until the SPI transaction is terminated by pulling CS low. The register sequence being followed is configurable via the SPI settings bits S1 and S0. Reading an invalid register address results in reading an infinite stream of zeros. If the read with clear command is used and a certain register has this feature, it will be cleared as soon as the data is transferred to the on-chip SPI shift register. This occurs on the rising clock edge of SCK that coincides with clocking out the MSB of that register on MISO. Any subsequent data bits not read will be lost, given that the register contents have already been cleared.

Write

Figure 23 illustrates a register write transaction. The header bits are followed by the data bits that need to be written to the register being addressed, MSB first. All writeable registers are 16 bits wide, so the header must be followed by 16 additional bits (D15-D0). Once the SA5301A has received these 16 data bits, they are written to the register. Subsequent sent data is ignored. An SPI write transaction can only perform a single write to a single register. If other registers need to be written as well, a new write transaction must be initiated. The data output MISO is floating throughout the entire write transaction. Writing to invalid addresses has no effect.

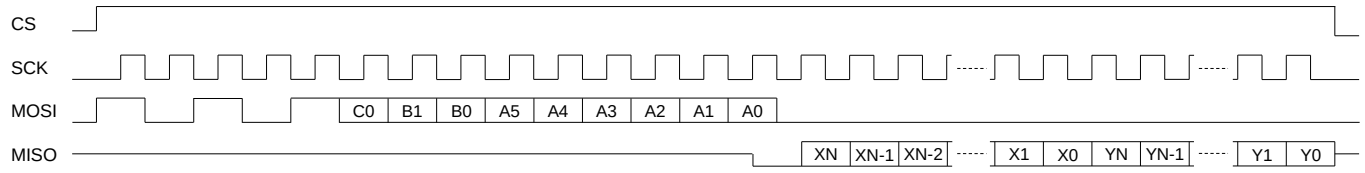


Figure 22: *SPI read transaction*

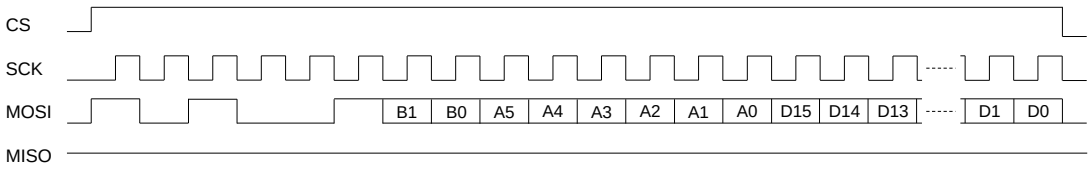


Figure 23: *SPI write transaction*

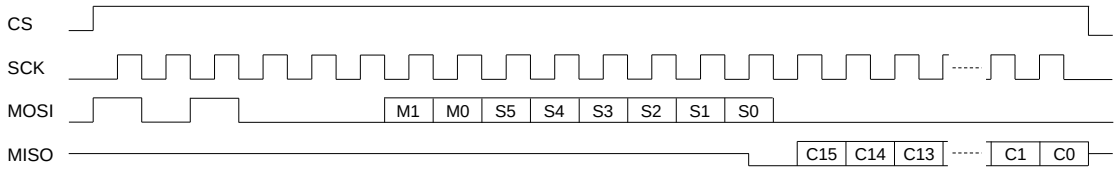


Figure 24: *SPI config transaction*

Config

The SPI config register command is used to access the SPI settings bits as well as the SPI CRC register that can be used to ensure data transfer integrity. The header format for the SPI config transaction is identical, although the bits have different meaning. Once the 8 config bits (M1, M0 and S5 to S0) have been received, the 16 CRC register bits (C15-C0) can be read out, see Figure 24. The CRC register does not cycle, all subsequent bits read beyond C0 will be zero.

SPI CRC Module

The SPI module contains a CRC feature to enable error checking of the SPI communication. The CRC-16-CCITT standard is used, which utilizes the polynomial $x^{16}+x^{12}+x^5+1$ (0x1021) with an initial value of 0xffff. Depending on the S4 settings bit the SPI header can be included during CRC computation, the register data being read or written is always included. During on-chip CRC computation, the sampled data on the MOSI pin is used for the header data as well as register write data. The data driven on the MISO pin is used for register read data. The CRC module operates on all transaction data, even accesses to invalid addresses. The CRC register can be read using the SPI config instruction. It will only be reset to the initial value if the M1 mode bit is set in the config instruction. The CRC data is never included in the CRC computation, although the header of the config instruction may be included, depending on the state of the S4 settings bit. The CRC module does not allow error correction, it only allows error detection of most communication errors.

DESIGN CONSIDERATIONS

Power Supplies

The SA5301A requires separate analog and digital power supplies. This allows the performance and the power consumption of the device to be optimized. The analog circuits should have a dedicated 5 V supply. Sharing this supply with digital circuitry should be avoided, as the supply noise created by digital switching activity might influence the analog circuits of the SA5301A. If this is unavoidable, then an LC based filter can be used to isolate the power supply noise from the SA5301A.

The power supply rejection ratio of the analog circuitry on the SA5301A is more than adequate to enable the circuitry to handle a few millivolt supply ripple. The supply ripple is, however, perfectly in phase with the mains voltage signals, so it will influence the energy measurement algorithms if it is too large.

Typically a low cost 5 V regulator like a 7805L or similar will provide an adequate analog supply for the SA5301A.

The digital supply can be shared with the digital supplies of the other components that make up the meter circuit, provided it is in the range 2.5 V to 5.5 V. This allows simple signal interfacing between the SA5301A and other devices. The suggested digital supply voltage is 3.3 V.

The analog and digital supply grounds need to be connected together. This should be done at a single point only, preferably by using a ferrite bead.

Bypass Capacitors

The analog and digital supplies and the VREF pin all require adequate bypass capacitance to reduce noise. The suggested value is 10 µF. The equivalent series resistance (ESR) of the bypass capacitors should be fairly low, so electrolytic capacitors should be avoided. A tantalum capacitor in parallel with a smaller ceramic capacitor or a single large ceramic capacitor is recommended instead.

Temperature Compensation

The SA5301A has been designed to have the lowest possible overall temperature coefficient. The external resistors in the voltage and current sensing networks and the ORES resistor can be a source of temperature variation if certain principles are not adhered to. Unless highest quality resistors are used, the external resistor values will always exhibit a relatively large temperature coefficient. It is recommended to use 1 % metal film resistors, which typically have a positive temperature coefficient in the order of 100 ppm °C/°, i.e. the resistance increases with temperature. It is possible to cancel this resistor temperature coefficient, to a first order approximation, if all external resistors

- are roughly at the same temperature and
- have similar temperature coefficients.

Usually this is achieved by selecting resistors from the same manufacturer and series, being aware of resistor power dissipation and careful PCB layout. Special attention should be given to the current transformer termination resistors. Very low value surface mount resistors often have different or unstable temperature coefficients compared to the rest of the

resistor series. The suggested solution is to use larger axial resistors for the CT termination, which tend to have a more controlled temperature coefficient.

Assuming the above principles have been adhered to the following deductions can be made (to a first order approximation and excluding any on-chip effects):

- The voltage sensing network is based on a voltage divider, so changes in temperature will not affect the input voltage on the voltage signal inputs.
- The current transformer termination resistors will increase with temperature, proportionally increasing the input voltage on the current signal inputs.
- The external resistor connected to ORES directly influences the oscillator frequency. The oscillator frequency is inversely proportional to the resistor value, so the oscillator frequency will tend to decrease as resistor value increases with temperature.
- The input impedance on the voltage and current signal inputs is inversely proportional to the oscillator frequency and thus directly proportional to the ORES resistor value. This input impedance interacts with the output impedance of the voltage and current sensing networks based on the voltage divider principle. A change in the output impedances of the sensing networks will therefore be cancelled by the similar change in the input impedance of the modulators.
- Referring to Equation (1) and Equation (2) it can be concluded that the directly proportional increase in input voltage on the current signal inputs will be cancelled by the inversely proportional decrease in oscillator frequency to produce a net zero change in register pulse rate.
- When considering current RMS and referring to Equation (3), the value of S_{RMS} will change with temperature as the input voltage on the current signal inputs changes. There is no counteracting variable in these equations, so current RMS exhibits an unavoidable directly proportional relationship to the CT termination resistor value.
- Changes in temperature do not affect the input voltage on the voltage signal inputs, so voltage RMS is stable with temperature.
- The mains period and phase angle register values are directly proportional to the oscillator frequency, so a temperature induced change in the ORES resistor value will affect the register values.

In order to achieve superior temperature compensation, it could be considered to tune the temperature coefficient of the ORES resistor to null any remaining temperature effects. The time reference register together with an accurate time base can also be used to perform similar compensation on a software level.

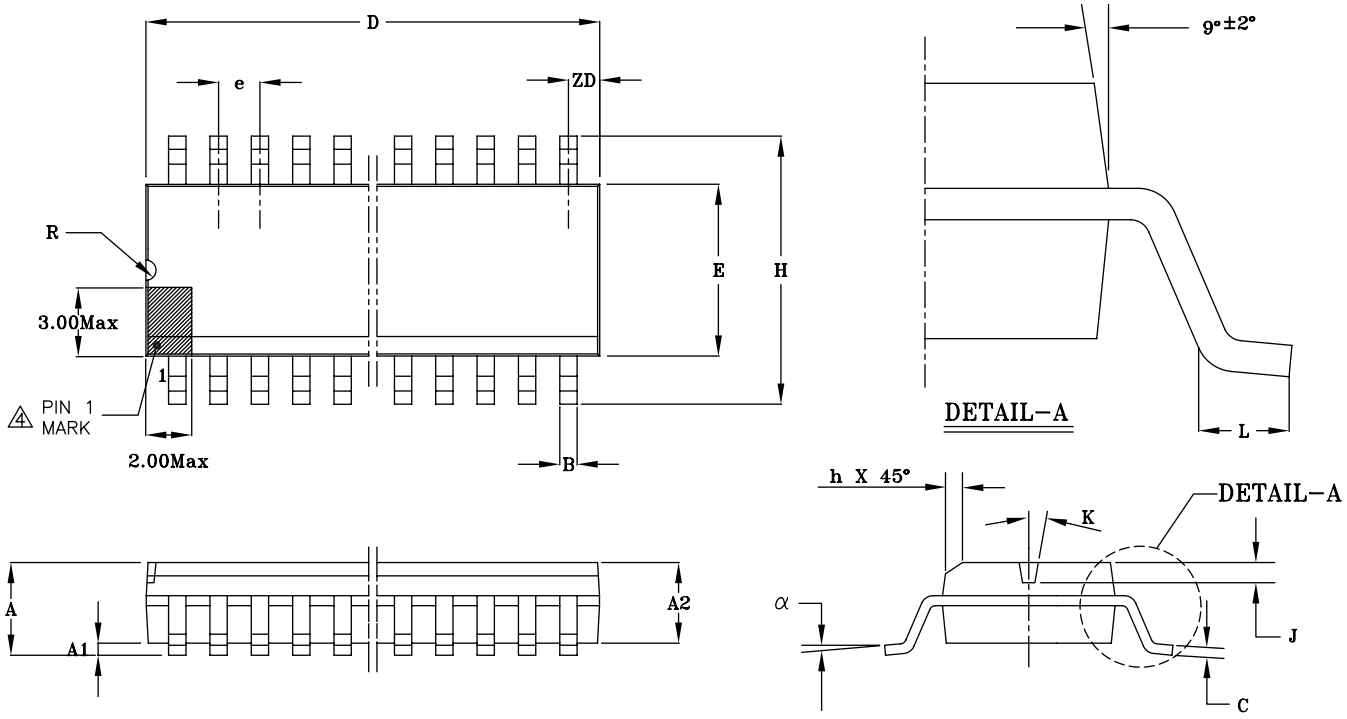
PCB Design

There are no critical considerations for designing the PCB layout, but the following principles should be incorporated to achieve optimal performance.

- Ground planes connected to the analog system ground should be used around and below the SA5301A and all the analog signals and components. The planes should be isolated from other ground planes used for other components to limit noise injection. Multiple vias should be placed to tie the top and bottom ground planes together. The use of a multi-layer PCB is not required, the pin layout of the SA5301A has been designed to enable efficient routing of all required signals on two layers.
- The wires and PCB traces from the current transformers to their termination resistors should form a closed loop of minimal area to prevent interference. The CT wires should be twisted, the PCB traces placed close together and surrounded by the ground plane. The PCB traces should be constrained to one routing layer if possible.
- The anti-alias filters of the voltage and current sensing networks, the CT termination resistors, the ORES resistor and the VREF and supply bypass capacitors should be as close as possible to the SA5301A.
- The current sensing networks are differential signal networks, care should be taken to keep their PCB layouts as symmetrical as possible.
- All external resistors associated with the SA5301A should be placed in the same region of the PCB. This ensures that they are subjected to similar temperature and improves temperature stability.

PACKAGE DIMENSIONS

SOIC24 Package



SYMBOL	SOIC-24LD MILLIMETERS	
	MIN	MAX
A	2.44	2.64
A1	0.10	0.30
A2	2.24	2.44
B	0.36	0.46
C	0.23	0.32
D	15.20	15.40
E	7.40	7.60
e	1.27 BSC	
H	10.11	10.51
h	0.31	0.71
J	0.53	0.73
K	7° BSC	
L	0.51	1.01
R	0.63	0.89
ZD	0.66 REF	
α	0°	8°

SYMBOL	SOIC-24LD INCHES	
	MIN	MAX
A	.096	.104
A1	.004	.012
A2	.088	.096
B	.014	.018
C	.0091	.0125
D	.598	.606
E	.291	.299
e	.050 BSC	
H	.398	.414
h	.012	.028
J	.021	.029
K	7° BSC	
L	.020	.040
R	.025	.035
ZD	.026 REF	
α	0°	8°

NOTES

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Any sales or technical questions may be sent to our support e-mail address:
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